Advancing GaN Power Device Technology:

Theoretical Insights into Reliability, Switching Behavior, and Device-Level Design Optimization

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Bodo's Wide Bandgap Event 2025

Making WBG Designs Happen

GaN

Outline



> GaN MISHEMT

Passivation
11 nm SiN cap
24 nm AlGaN Barrier
310 nm GaN Channel

Buffer

Substrate

Breakdown voltage > 650 V

Intrinsic failure mechanisms: Current collapse, Dynamic Ron

> CAVET

Gate

Gate

AlGaN

UID GaN channel

CBL

Aperture
Length

CBL

n- GaN drift layer
n+ GaN substrate

Drain

Source

Source

Oxide

n- GaN drift layer

Drain

p GaN

Static & Dynamic characteristic

Application prospective

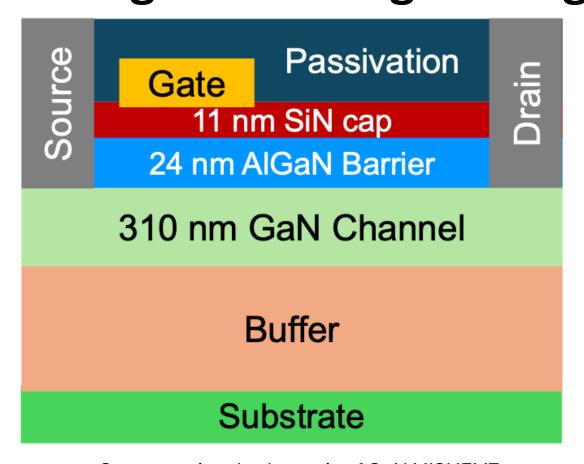
> Trench MOSFET

static and dynamic optimization, Switching loss, Power loss

Advanced Design



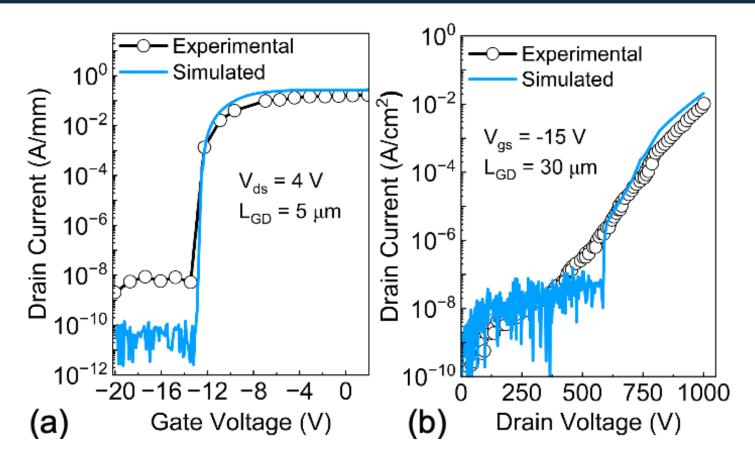
Improving Thermal and Electrical Performance of AlGaN/GaN MISHEMTs through Buffer Engineering



Cross-sectional schematic of GaN MISHEMT.

Calibration of the Fabricated GaN MISHEMT with SiN-stack

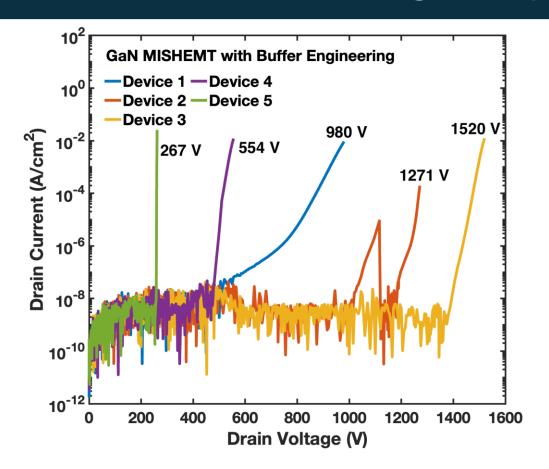


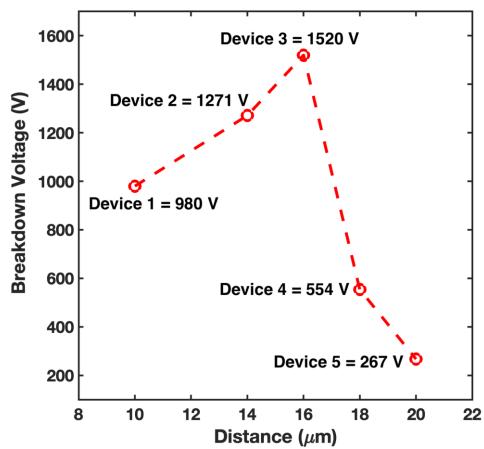


Calibrated (a) DC transfer characteristics at gate-drain distance of 5 µm , and (b) Off-state breakdown voltage at gate-drain distance of 30 µm of fabricated GaN MISHEMT device

Breakdown Voltage analysis of different devices



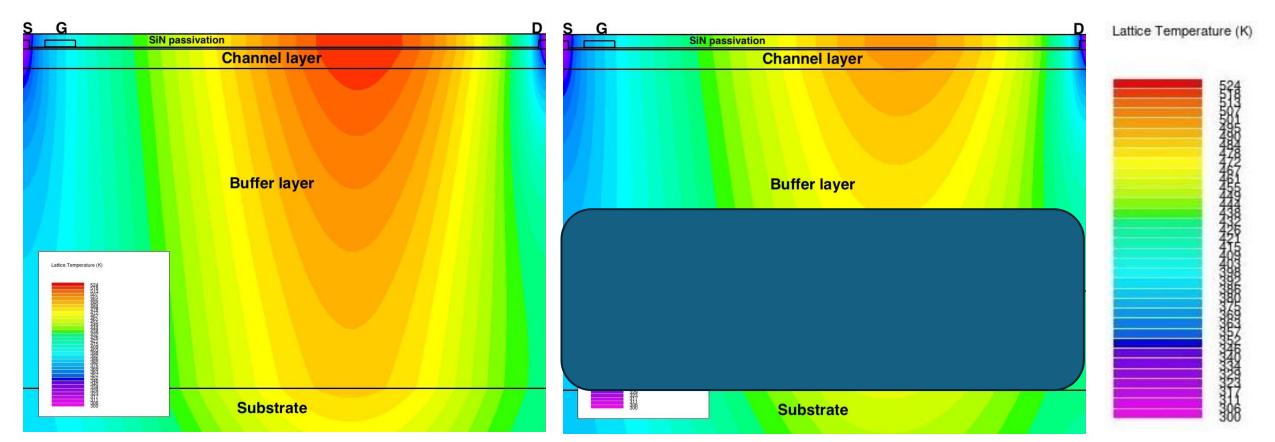




Breakdown Voltage analysis of different devices

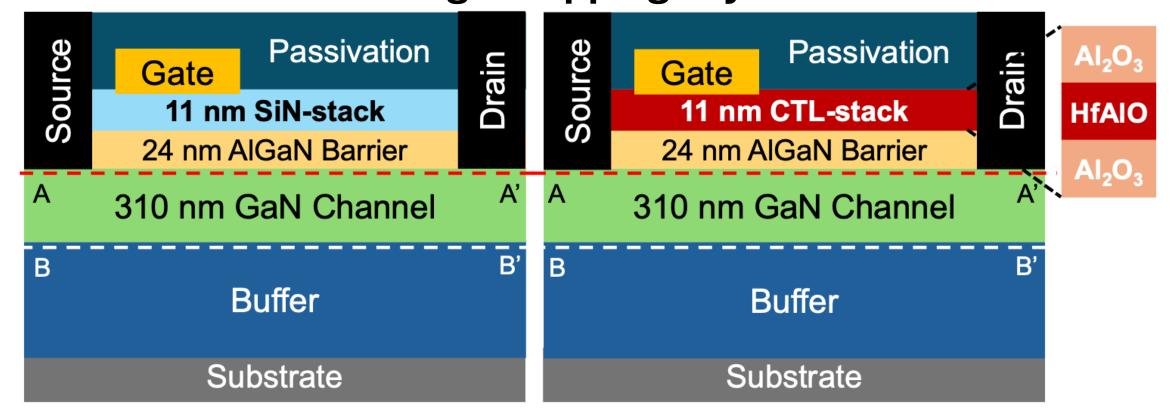
Normalized Self-heating Effect at 524 K





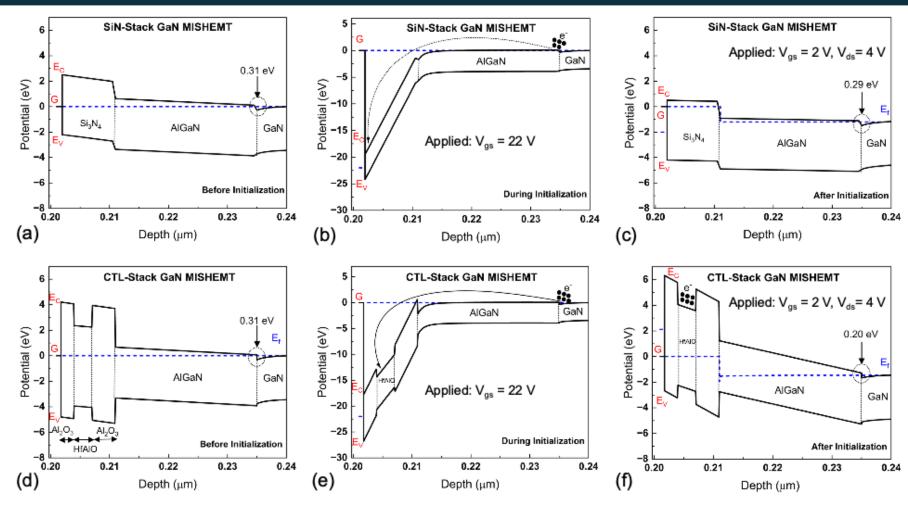


Mitigation of Current Collapse and Dynamic RON in GaN MISHEMTs Using a Quantum-Well-Engineered Al2O3/HfAlO/Al2O3 Charge-Trapping Layer



Schematic Band Diagram of GaN MISHEMTs





Simulated schematic band diagram at the gate region of the GaN MISHEMT with SiN-stack (a) before, (b) during, and (c) after initialization process, and the GaN MISHEMT with CTL-stack (d) before, (e) during, and (f) after initialization process, respectively.

I-V Characteristics of GaN MISHEMTs



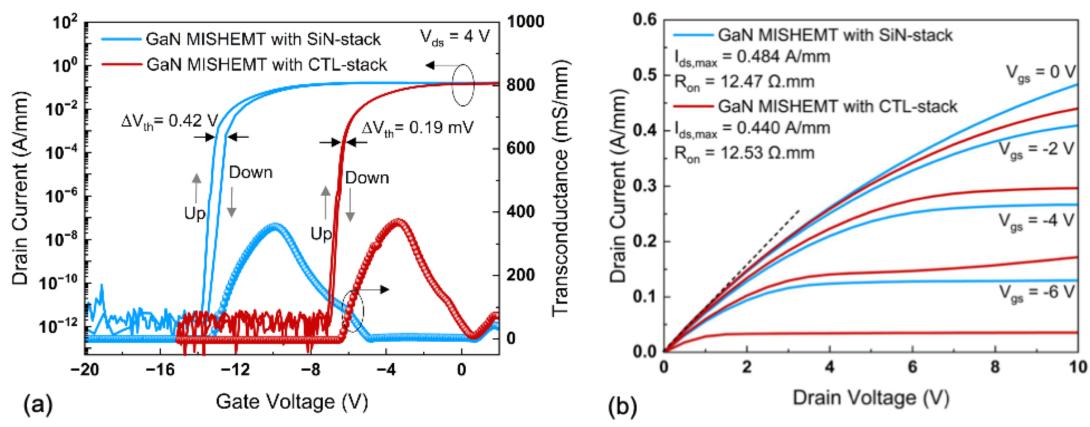
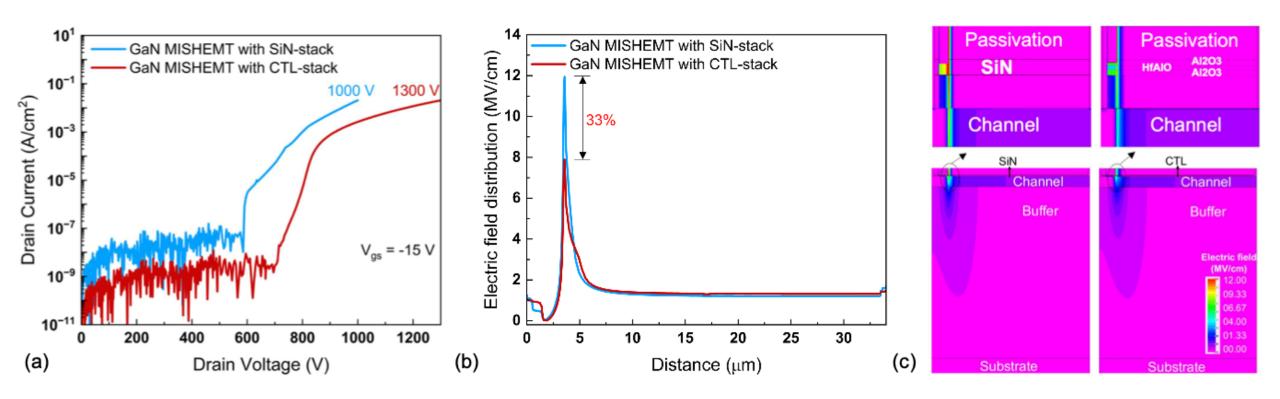


Fig. 4. (a) Dual sweep transfer characteristics, and (b) output characteristics of the devices.

Breakdown Characteristics of GaN MISHEMTs

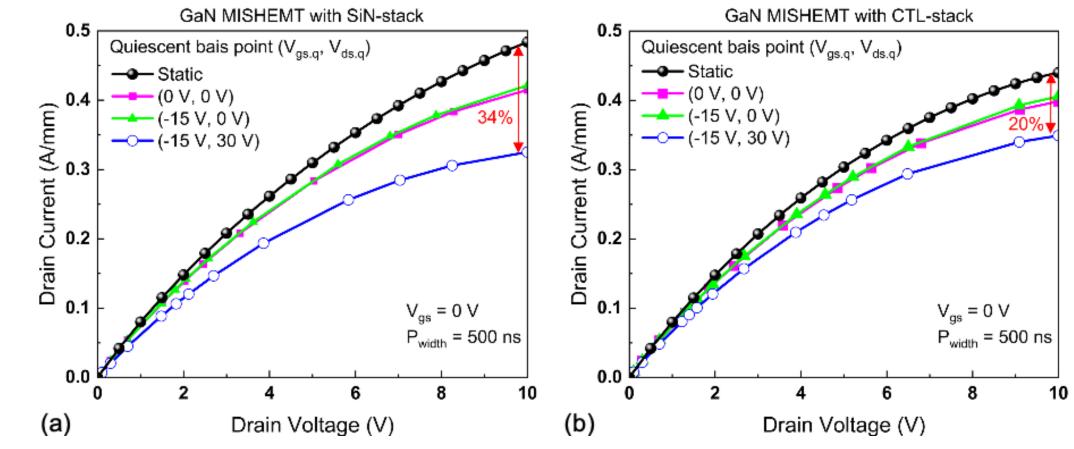




(a) Breakdown voltage characteristics at Vgs = -15 V, (b) electric-field distribution at Vds of 500 V, and (c) comparison of the computed electric field distribution of the MISHEMT devices.

Current Collapse Characterization of GaN MISHEMTs

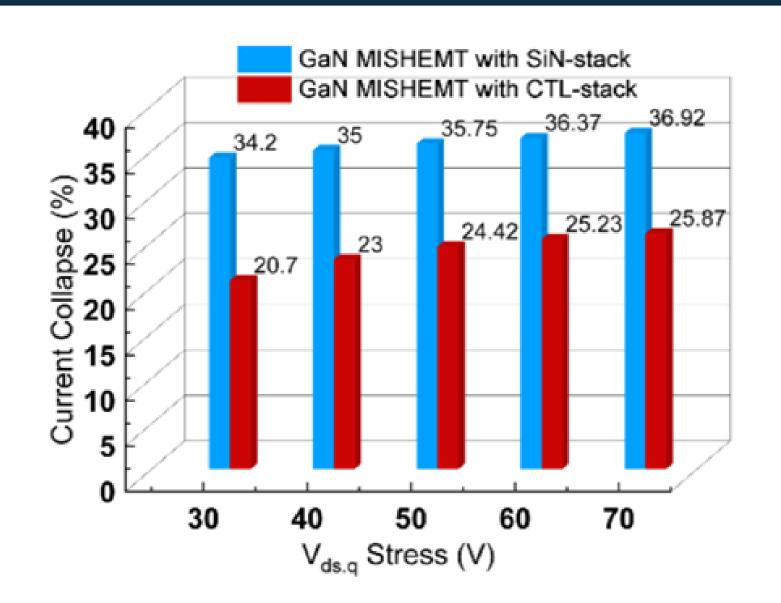




Pulsed I–V characteristics of GaN MISHEMT with (a) SiN-stack and (b) CTL-stack device and (c) Current collapse ratio at Vgs = 0 V, Vds = 10 V with different quiescent bias over static bias.

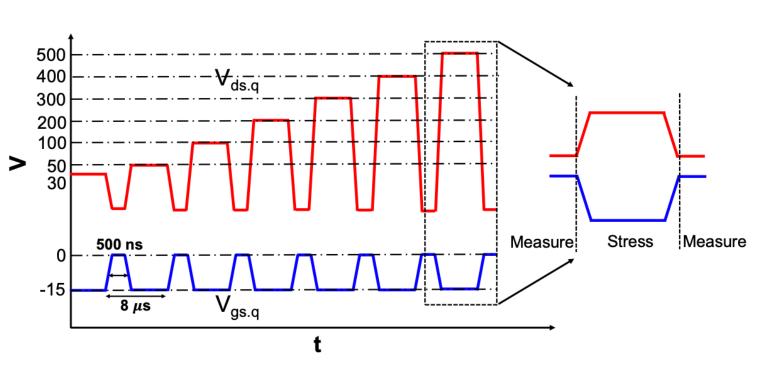
Dependency of Current Collapse Effect



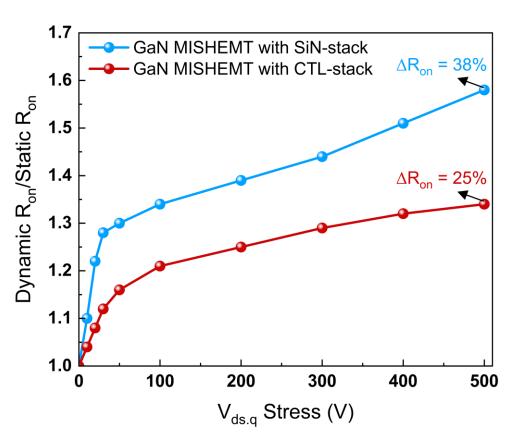


Dynamic Ron Characterization of GaN MISHEMTs





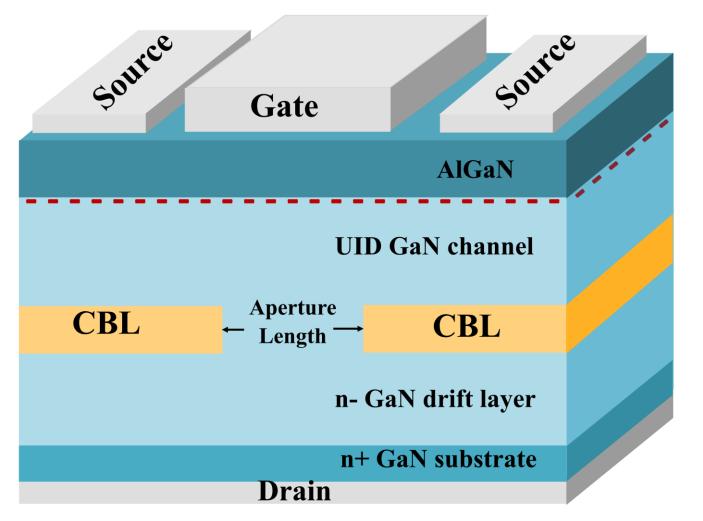
Timing diagram depicting describing the measure-stress-measure cycle.



Dynamic RON degradation of both devices.

Current Aperture Vertical Electron Transistor (CAVET)

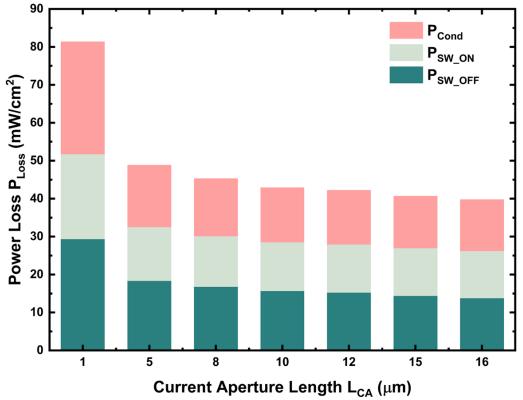




Conventional CAVET Structure

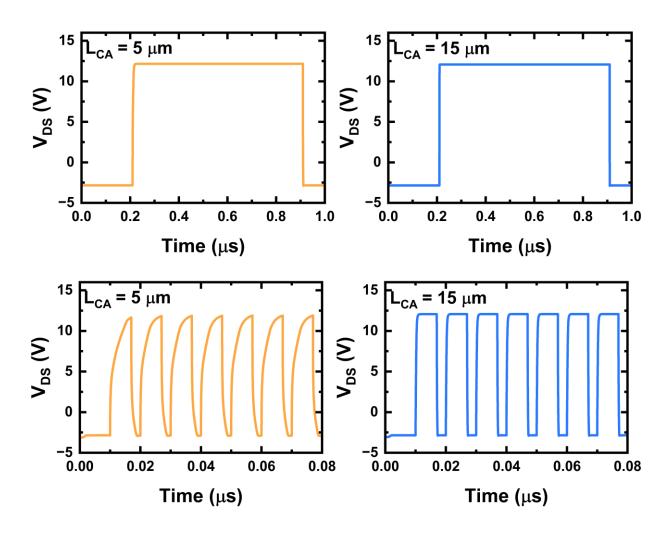
By optimizing aperture length

- The turn-on and turn-off power losses decreased by 53% and 45%.
- Total loss is reduced almost by half.

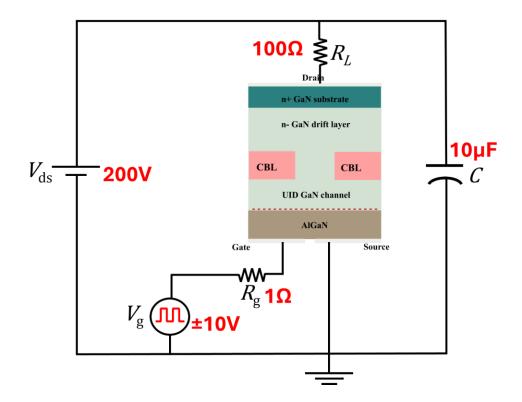


Applications (Oscillator)





■ The output waveform of the oscillator remains sharp for larger aperture length at higher frequencies.

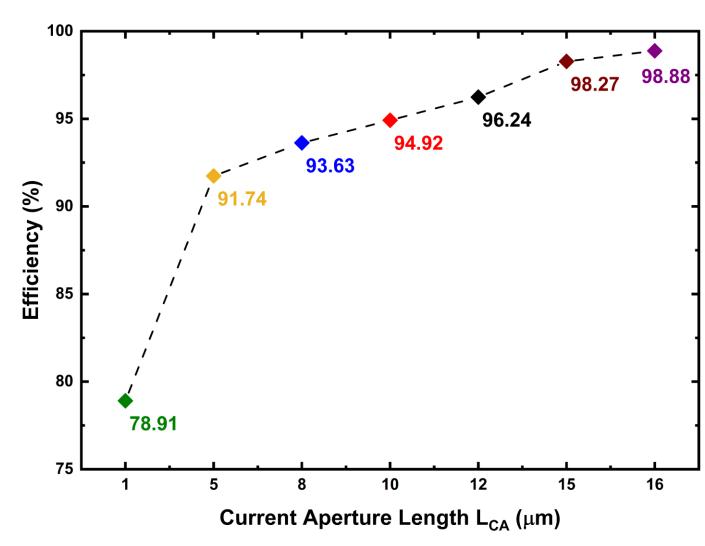


Typical waveforms of CAVET in the rectangular-wave oscillator circuit at switching frequencies of 1 MHz and 100 MHz.

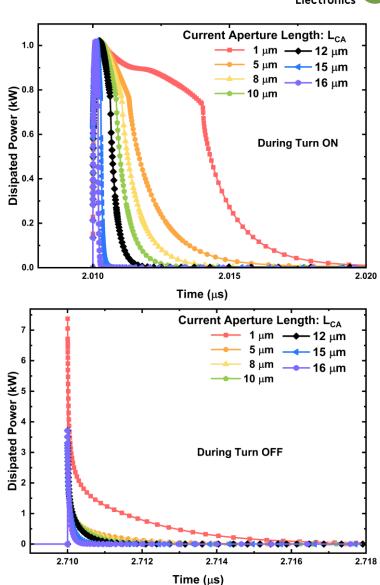
Schematic circuit diagram of a rectangular-wave oscillator circuit

Applications (DC-DC Boost Converter)





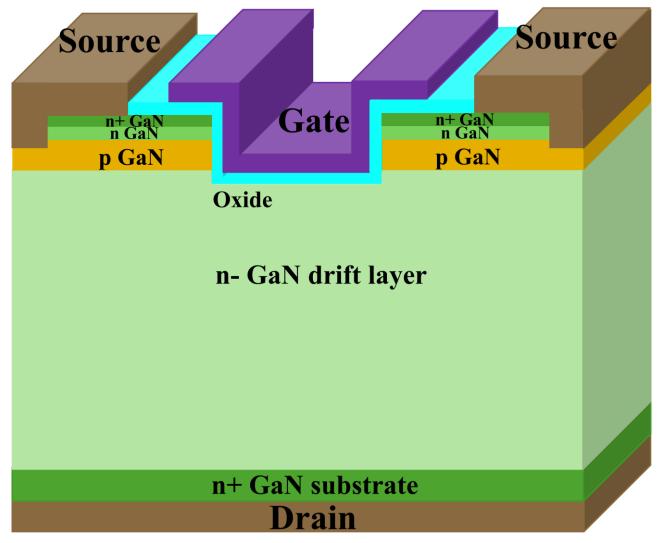
Efficiency of DC-DC Boost Converter Circuit with CAVET switch.



The dissipated power during the turn-on and off in the DC-DC Boost Converter.

Vertical GaN TMOS



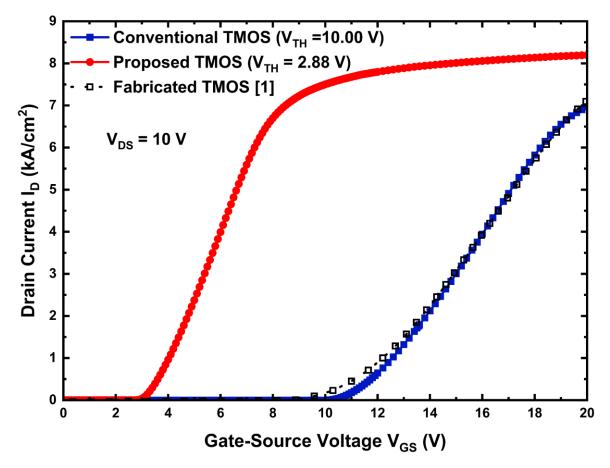


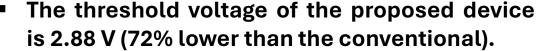
Conventional Vertical GaN TMOS Structure

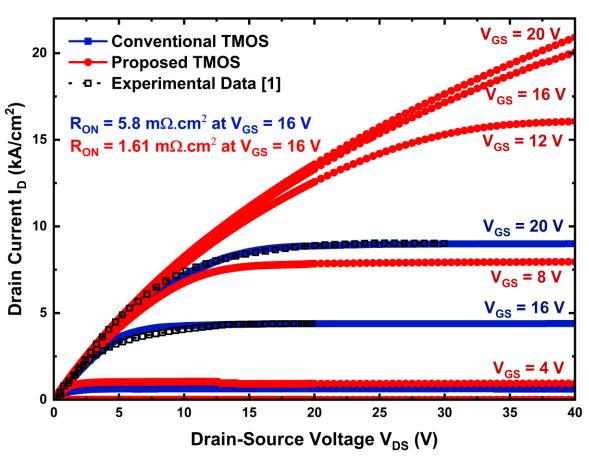
[1] M. Kamiński, A. Taube, J. Tarenko, O. Sadowski, E. Brzozowski, J. Wierzbicka, M. Zadura, M. Ekielski, K. Kosiel, and J. Jankowska-Śliwińska, "Verţical GaN Trench-MOSFETs Fabricated on Ammonothermally Grown Bulk GaN Substrates," physica status solidi (a), pp. 2400077, 2023.

Proposed TMOS (Static Characteristics)







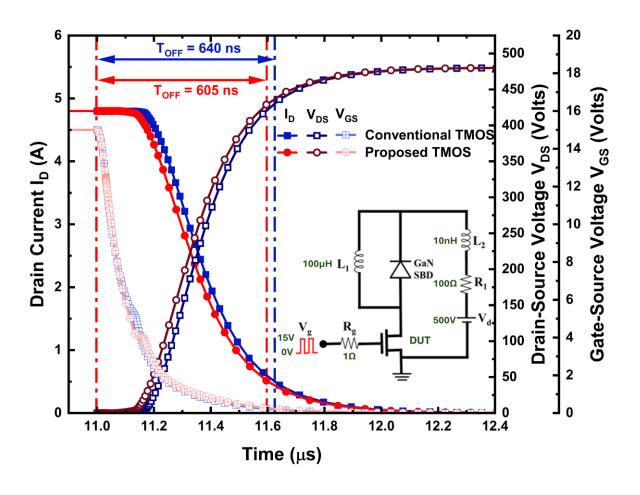


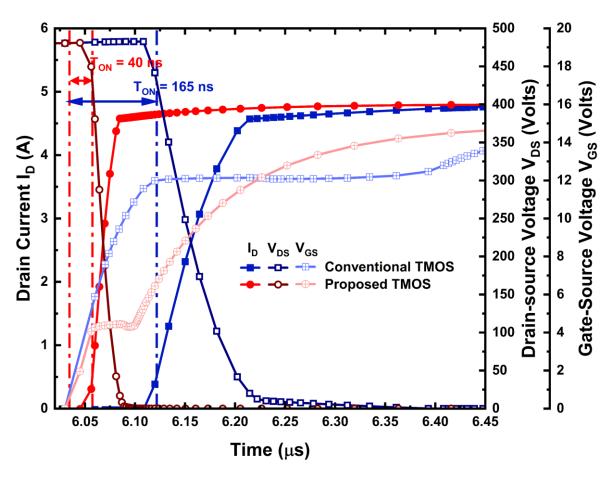
- The output current is 2 times higher than that of the conventional device.
- The on-state resistance is 70% lower than the conventional TMOS.

[1] M. Kamiński, A. Taube, J. Tarenko, O. Sadowski, E. Brzozowski, J. Wierzbicka, M. Zadura, M. Ekielski, K. Kosiel, and J. Jankowska-Śliwińska, "Verţical GaN Trench-MOSFETs Fabricated on Ammonothermally Grown Bulk GaN Substrates," physica status solidi (a), pp. 2400077, 2023.

Proposed TMOS (Switching Characteristics)





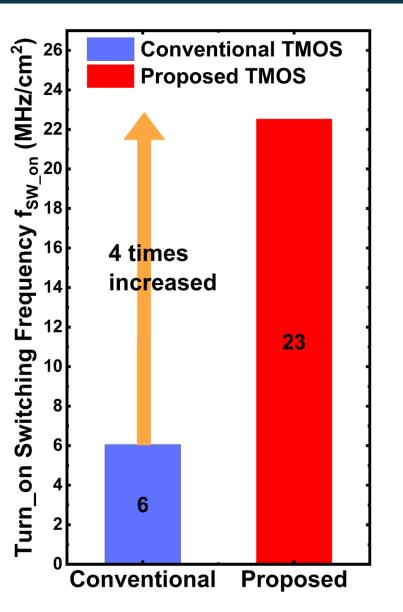


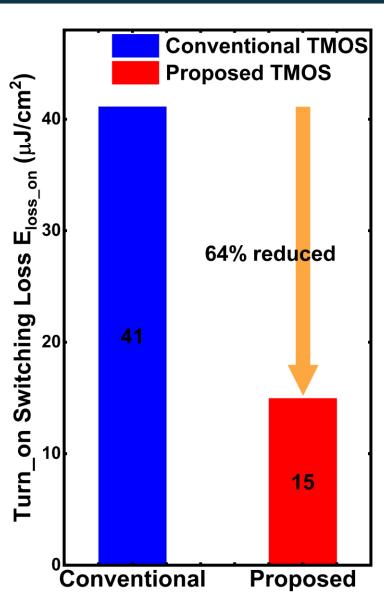
Turn-off time is 35 ns lower than the conventional TMOS

Turn-on time decreases more than 4 times.

Proposed TMOS (Switching Characteristics)



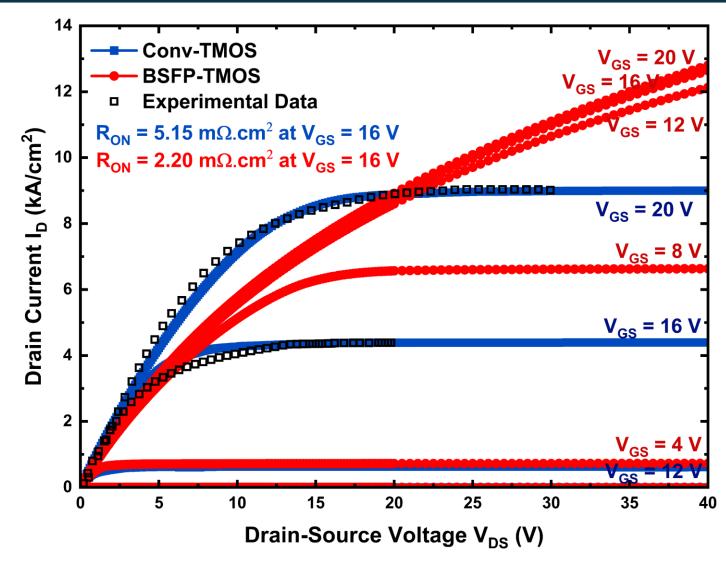




- The turn-on switching frequency is four times higher than the conventional TMOS.
- The turn-on switching loss is reduced by 64%.

Advanced Design for TMOS



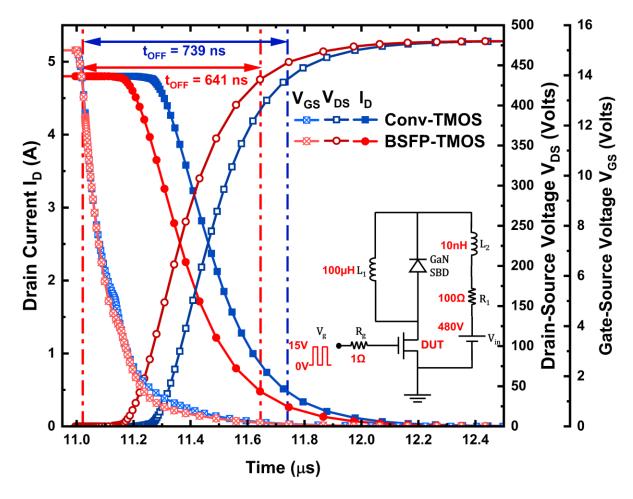


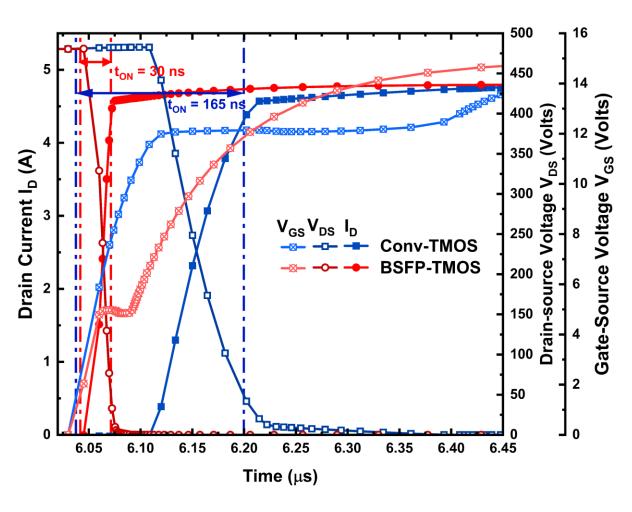
Output Characteristics

- The output current increases from 9 kA/cm² to 13 kA/cm².
- The on-state resistance is 60% lower than the conventional TMOS.

Advanced Design for TMOS (Switching Characteristics)





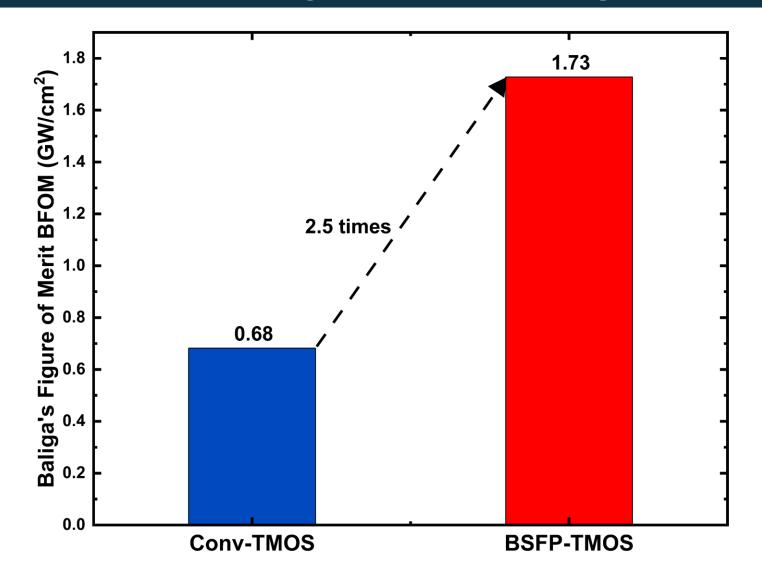


Turn-off time is 98 ns lower than the conventional TMOS

Turn-on time decreases more than 5 times.

Advanced Design for TMOS (Figure of Merits)





 Baliga Figure of Merit increases by approximately 3 times.

THANK YOU!