Improving GaN Model Accuracy

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Bodo's Wide Bandgap Event 2025

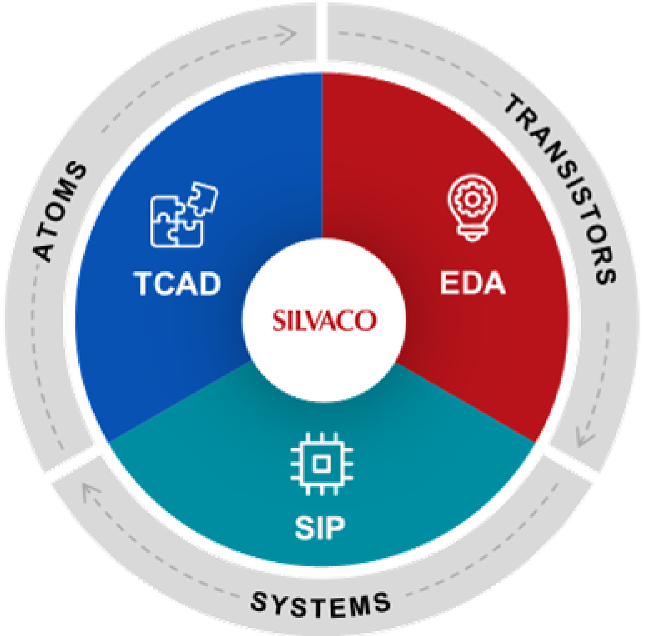
Making WBG Designs Happen

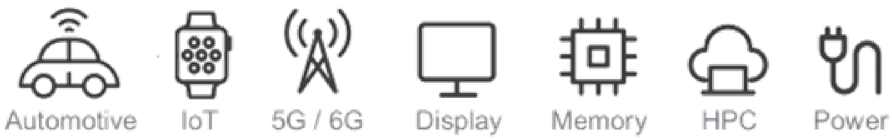
GaN

Silvaco at a Glance

Enabling semiconductor innovation from atoms to systems

Design, Simulate, Analyze, and Verify from Concept to Complete Product Yield





ISO 9001 CERTIFIED by schellman

Silvaco Leadership

8 of 10(1) Largest Display Companies Use Silvaco's TCAD

4 of 10(4) Largest SiC, GaN Power Device Providers Use Silvaco TCAD

6 of 10(3) Largest Semiconductor Companies Use Silvaco's EDA

800+ (2) Customers

200+ University Customers

400+(5) Employees

Global Presence

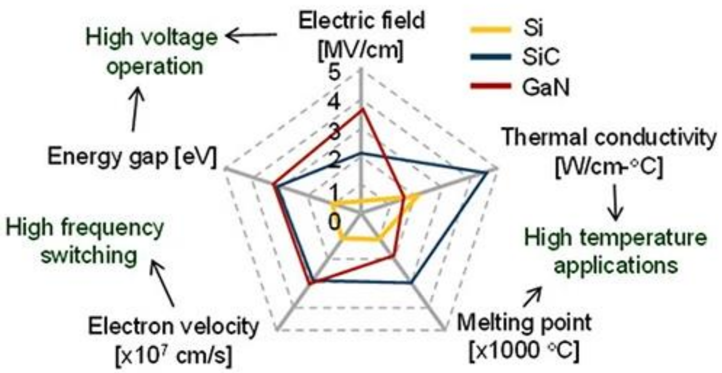
1) Largest in terms of revenue from Q4'2023 to Q3 2024 according to Counterpoint Research
2) Data as of September 30, 2024
3) Largest in terms of revenue according to companiesmarketcap.com
4) 2024 Future Market Insight SiC and GaN Semiconductor Market Report
5) Data as of August 2025

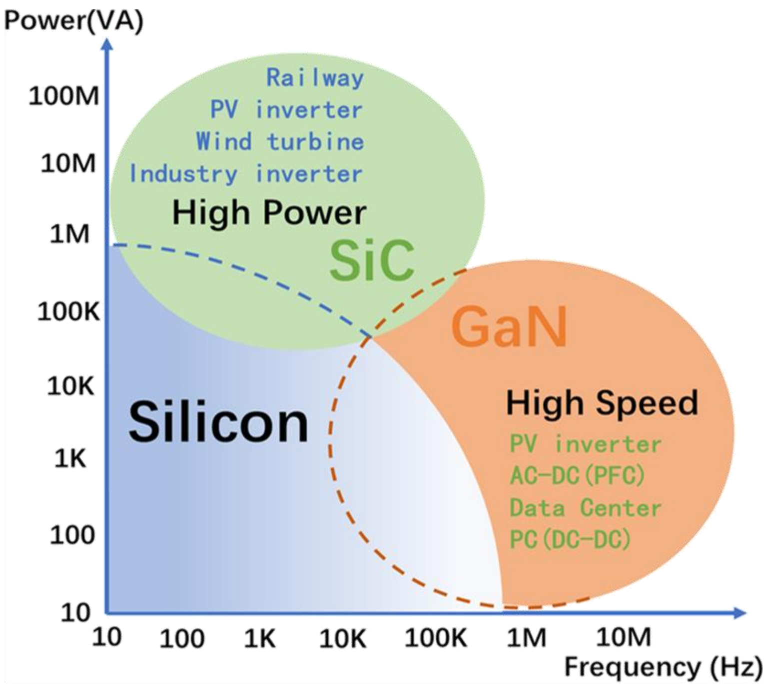
Outline

- GaN for Power Electronics
  - The GaN Technology Landscape
- Role of TCAD in GaN HEMT Design
- Role of AI in Power Electronics
  - Silvaco Victory Platform solution
- Case Study: Vertical GaN Device (CAVET)
  - Silvaco for AI-driven Device Optimization
  - Exploring Yield With ML Model
- Summary

GaN for Power Electronics

Advantages over Si and SiC, and Challenges





- Gate Reliability & Threshold Stability
- Substrate Quality & Defect Density
- Thermal Management
- Process Integration

The GaN Technology Landscape

Topologies	Architecture	Key Features
Normally-On (Depletion-Mode)	D-Mode AlGaN/GaN HEMT	Simple heterostructure, high 2DEG density Lowest RDS(on) for given die size Requires negative gate bias or cascode to make failsafe
	D-Mode GaN MISHEMT	
Normally-Off (Enhancement-Mode)	p-GaN Gate HEMT	Safer “off at 0 V” behavior Easy to drive with standard gate drivers (±6 V typical) Slightly higher RDS(on)
	MISHEMT	
Novel / Vertical / Advanced	Vertical GaN FET	True vertical current path Targeting EV traction inverters, renewables, industrial drives
	FinFet / Tri-Gate GaN	
	Trench-Gate GaN	

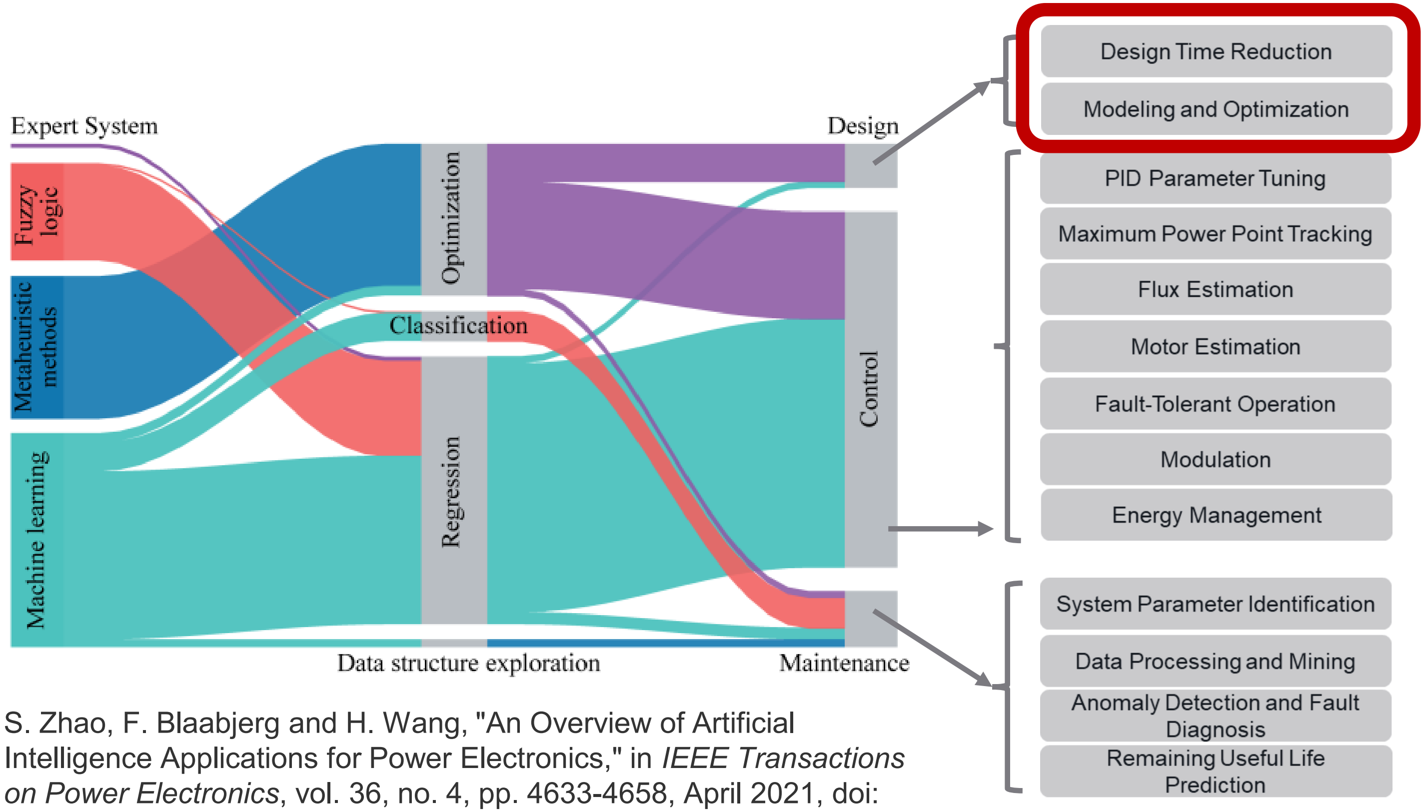
GaN HEMT – A complex device physics

- Polarization charge
- Bulk traps – AlGaN/GaN stack
- Interface Traps – p-gaN/AlGaN
- Interface Traps – AlGaN/Nitride
- Metal Workfunction
- Electron/Hole mobility along AlGaN/GaN interface (2DEG)
- Substrate stack – Epi thickness and temperature

Use TCAD and Design of Experiments (DOE) to analyze their impact on device's electrical behavior to master device design!

Artificial Intelligence for Power Electronics

Design Time Reduction and Optimization



S. Zhao, F. Blaabjerg and H. Wang, "An Overview of Artificial Intelligence Applications for Power Electronics," in *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4633-4658, April 2021, doi: 10.1109/TPEL.2020.3024914.

Power electronic design process stages and estimated time.

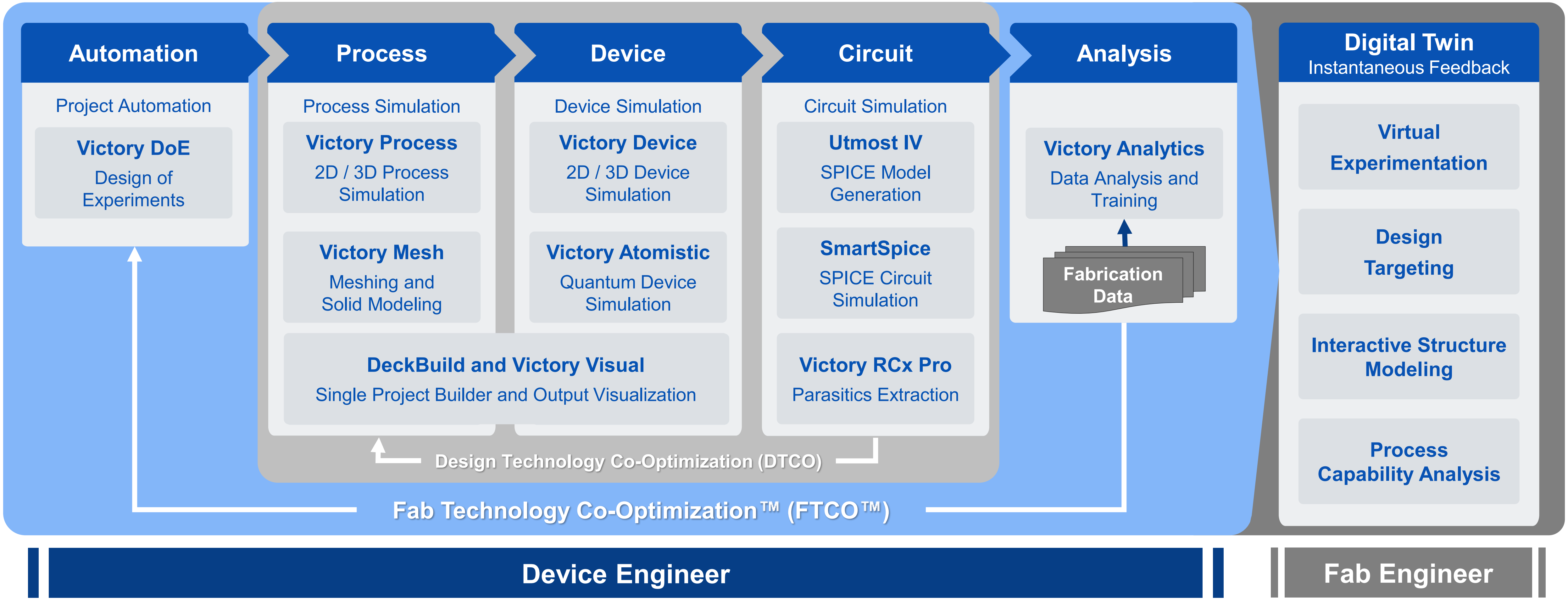
Electronic design process stage	Estimated time (weeks)
Conceptual design	0–4
Design Specification	1–6
Computation/Mathematical modelling	1–8
Simulation	1–12
[illegible]	[illegible]
Prototyping (PCB layout, Schematic design, Component selection)	4–12
Code/Software development	1–8
Hardware testing and debugging	2–12
Set up, integration and system testing	4–8
Certification and compliance testing	4–8
Final prototyping and validation	6–10
Mass production	Ongoing (months)

Khalifa Aliyu Ibrahim, et al., Revolutionizing power electronics design through large language models: Applications and future directions, Computers and Electrical Engineering, Volume 123, Part D, 2025, 110248, https://doi.org/10.1016/j.compeleceng.2025.110248

Design Time Reduction for Device Modeling and Optimization is vital to develop advanced technological solutions

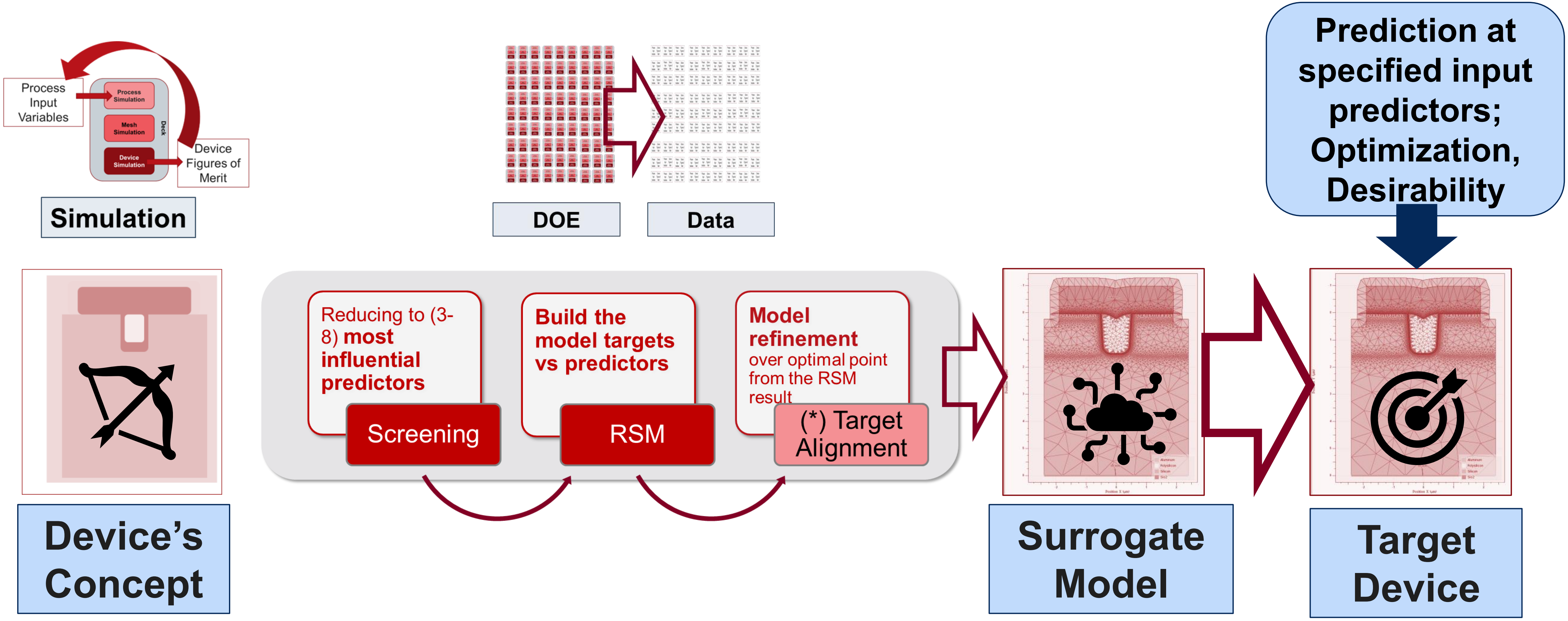
Victory TCAD Platform

Develop Semiconductor Processes and Devices Prior to and During Manufacturing



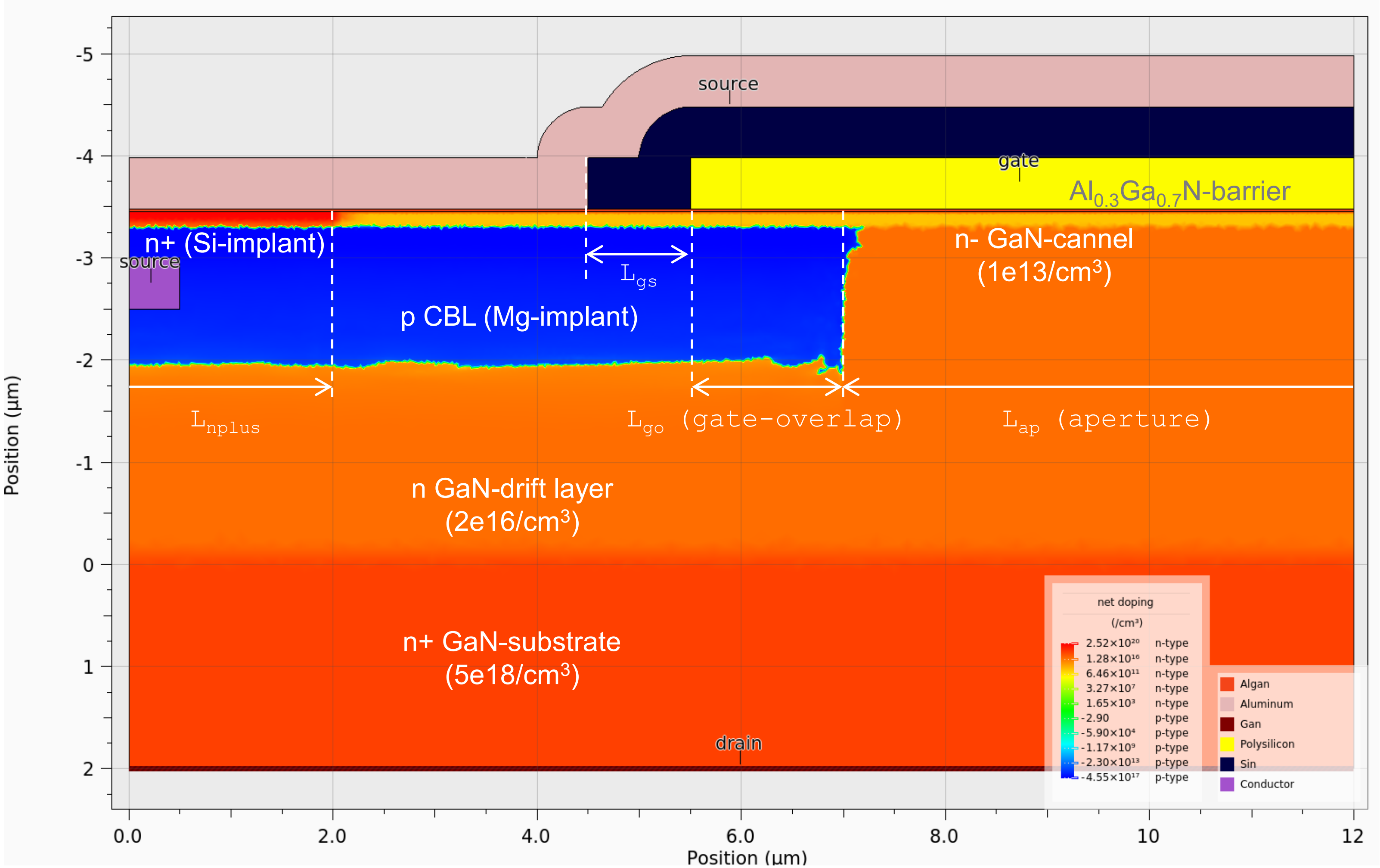
Surrogate Models from TCAD Simulations

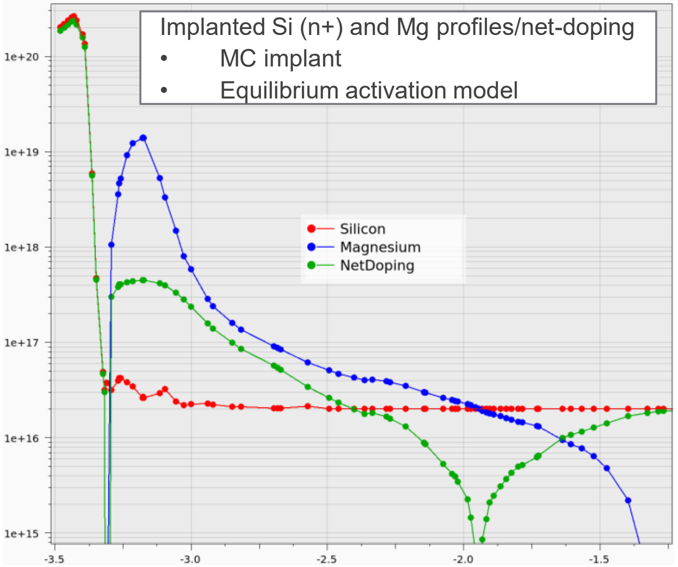
SILVACO Victory Flow for Device Optimization over Surrogate Models

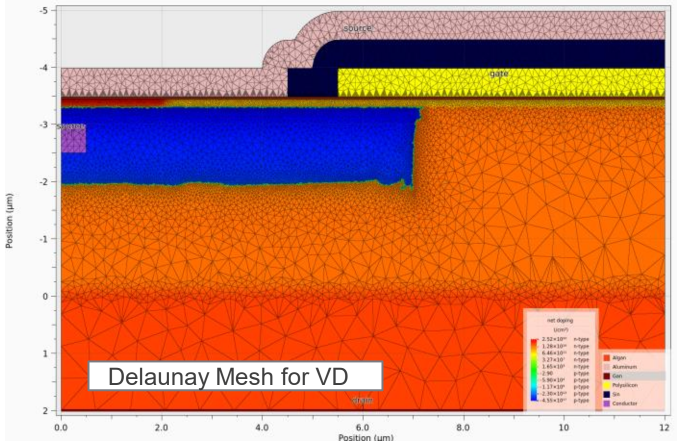


Vertical GaN Device (CAVET)

Process simulation structure (doping profile)





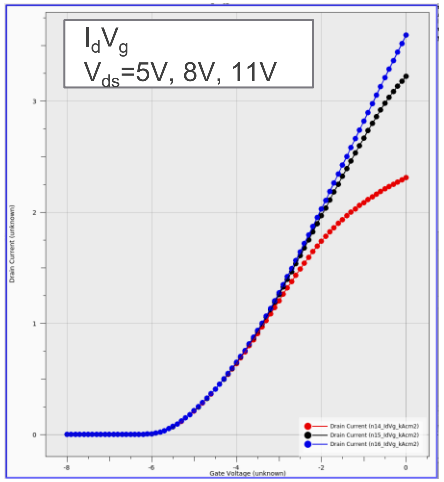


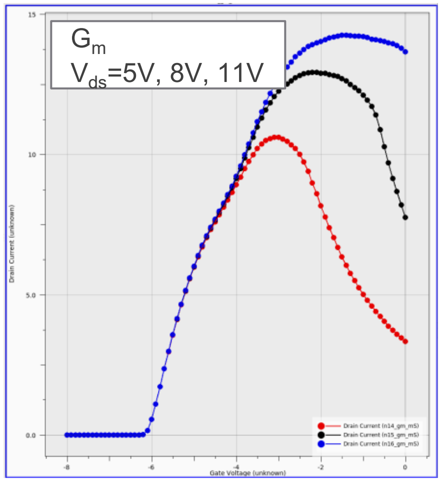
Victory DoE Deck and IV Curves

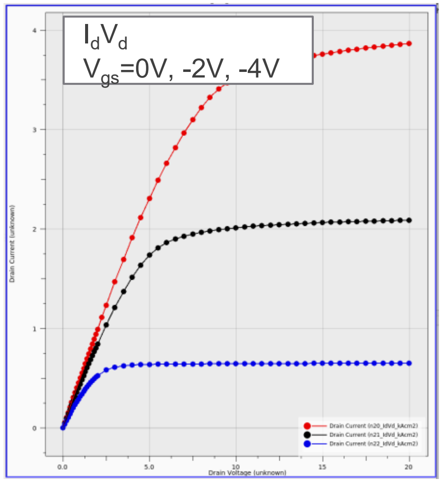
Victory Process / Victory Device

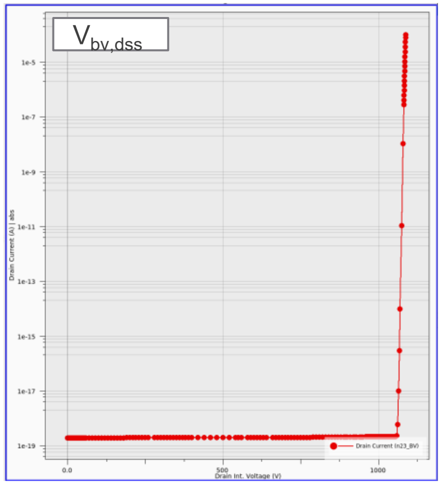
Dashboard | DOE | Node | Time | Memory | Elements

Row	Module	Variable	1	2	3	4	5	6	7	8	9
1	GlobalVar		n1	n1	n1	n1	n1	n1	n1	n1	n1
2	Epitaxy		n2	n2	n2	n2	n2	n2	n2	n2	n2
		epi_doping	2e+16	2e+16	2e+16	2e+16	2e+16	2e+16	2e+16	2e+16	2e+16
3	CBL		n3	n3	n3	n3	n3	n3	n3	n3	n3
		Lap_um	10	10	10	10	10	10	10	10	10
		cbl_energy	80	80	80	80	80	80	80	80	80
4	Regrowth		n4	n4	n4	n4	n4	n4	n4	n4	n4
5	Barrier		n5	n5	n5	n5	n5	n5	n5	n5	n5
6	NPlus		n6	n6	n6	n6	n6	n6	n6	n6	n6
7	Anneal		n7	n7	n7	n7	n7	n7	n7	n7	n7
8	PolyGate		n8	n8	n8	n8	n8	n8	n8	n8	n8
		Lgo_um	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
9	Electrode		n9	n9	n9	n9	n9	n9	n9	n9	n9
		Lgs_um	1	1	1	1	1	1	1	1	1
10	Remeshing		n10	n10	n10	n10	n10	n10	n10	n10	n10
		Temperature_C	25	25	25	25	25	25	25	25	25
11	Threshold		n11	n11	n11	n12	n12	n12	n13	n13	n13
		Vds_V	5	5	5	8	8	8	11	11	11
12	Vth		n14	n14	n14	n15	n15	n15	n16	n16	n16
13	Output		n17	n18	n19	n17	n18	n19	n17	n18	n19
		Vgs_V	0	-2	-4	0	-2	-4	0	-2	-4
14	Rdson		n20	n21	n22	n20	n21	n22	n20	n21	n22
15	Breakdown		n23	n23	n23	n23	n23	n23	n23	n23	n23
		BV_IdVd	1	1	1	1	1	1	1	1	1
		Capacitance	0	0	0	0	0	0	0	0	0
16	Vbrdss		n24	n24	n24	n24	n24	n24	n24	n24	n24

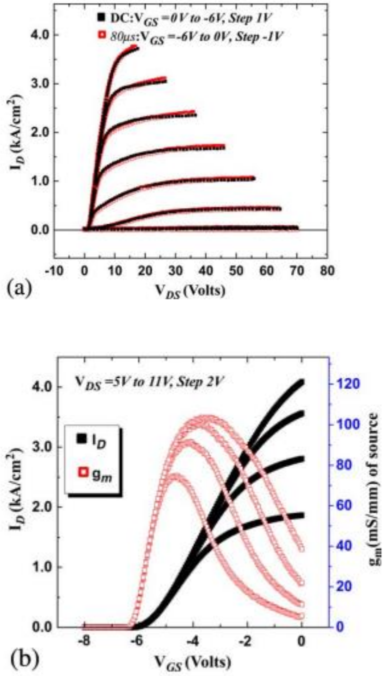








Chowdhury *et. al*, IEEE ELECTRON DEVICE LETTERS, VOL. 33, NO. 1, JANUARY 2012

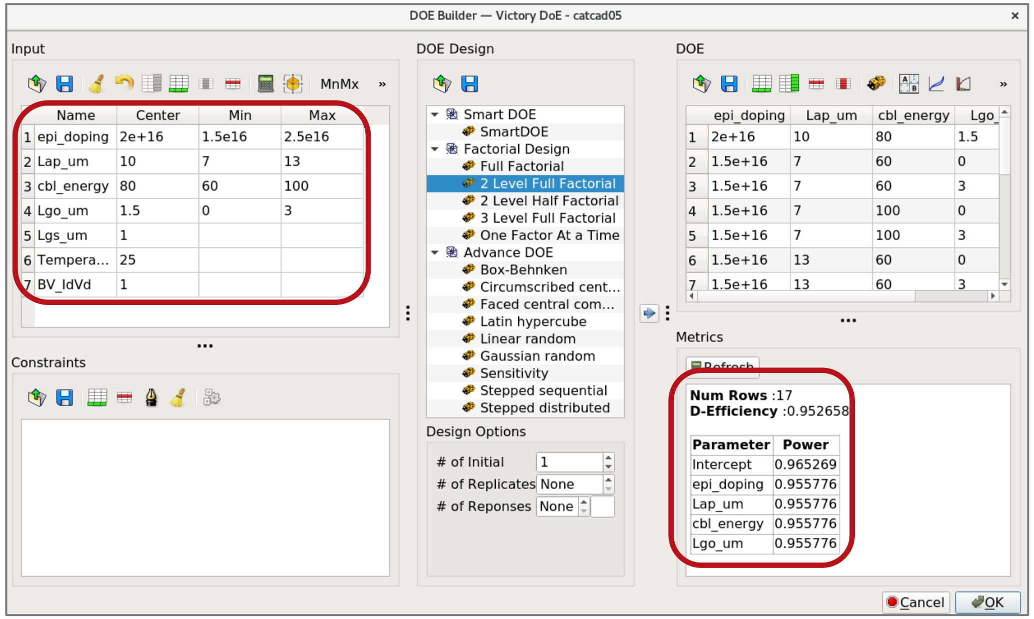


Select Dominant Model Parameters

Decision Forest Selection – Victory Analytics

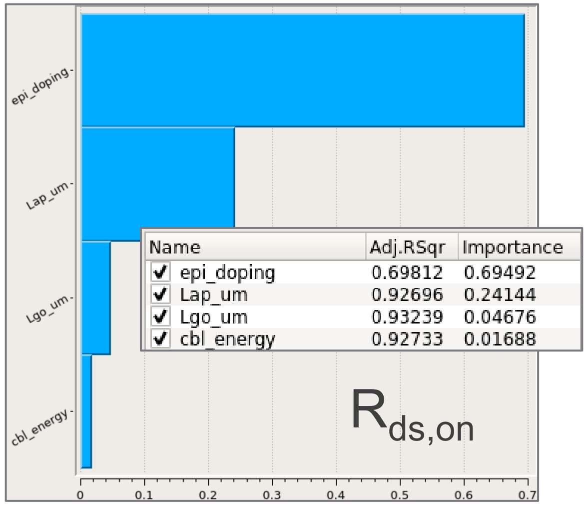
Sensitivity analysis in Victory DoE

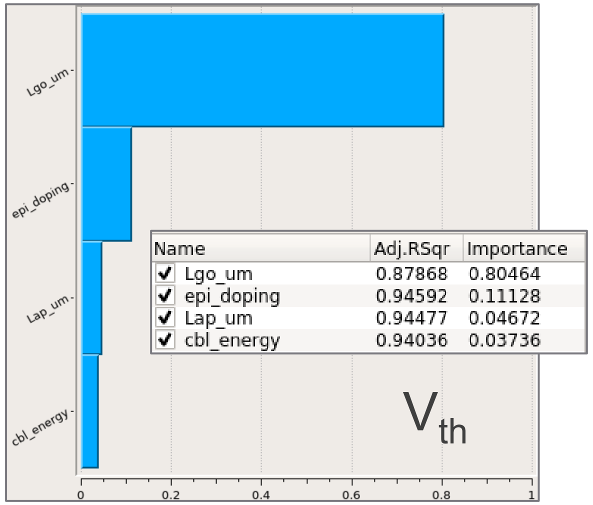
- 2-Level full factorial
  - 4 parameters: $2^4 + 1 = 17$ simulations
- Select parameters
  - Down-select from 4 to 3 parameters
  - Sensitivity w/r to $R_{ds,on}$ and V_{th}



Dashboard | DOE | Node | Time | Memory | Elements

Row	Module	Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	GlobalVar		n1	n1	n1	n1	n1	n1	n1	n1	n1	n1	n1	n1	n1	n1	n1	n1	n1
2	Epitaxy		n2	n3	n3	n3	n3	n3	n3	n3	n3	n4	n4	n4	n4	n4	n4	n4	n4
		epi_doping	2e+16	1.5e+16	1.5e+16	1.5e+16	1.5e+16	1.5e+16	1.5e+16	1.5e+16	1.5e+16	2.5e+16	2.5e+16	2.5e+16	2.5e+16	2.5e+16	2.5e+16	2.5e+16	2.5e+16
3	CBL		n5	n6	n6	n7	n7	n8	n8	n9	n9	n10	n10	n11	n11	n12	n12	n13	n13
		Lap_um	10	7	7	7	7	13	13	13	13	7	7	7	7	13	13	13	13
		cbl_energy	80	60	60	100	100	60	60	100	100	60	60	100	100	60	60	100	100
4	Regrowth		n14	n15	n15	n16	n16	n17	n17	n18	n18	n19	n19	n20	n20	n21	n21	n22	n22
5	Barrier		n23	n24	n24	n25	n25	n26	n26	n27	n27	n28	n28	n29	n29	n30	n30	n31	n31
6	NPlus		n32	n33	n33	n34	n34	n35	n35	n36	n36	n37	n37	n38	n38	n39	n39	n40	n40
7	Anneal		n41	n42	n42	n43	n43	n44	n44	n45	n45	n46	n46	n47	n47	n48	n48	n49	n49
8	PolyGate		n50	n51	n52	n53	n54	n55	n56	n57	n58	n59	n60	n61	n62	n63	n64	n65	n66
		Lgo_um	1.5	0	3	0	3	0	3	0	3	0	3	0	3	0	3	0	3
9	Electrode		n67	n68	n69	n70	n71	n72	n73	n74	n75	n76	n77	n78	n79	n80	n81	n82	n83
10	Remeshing		n84	n85	n86	n87	n88	n89	n90	n91	n92	n93	n94	n95	n96	n97	n98	n99	n100
11	Threshold		n101	n102	n103	n104	n105	n106	n107	n108	n109	n110	n111	n112	n113	n114	n115	n116	n117
12	Vth		n118	n119	n120	n121	n122	n123	n124	n125	n126	n127	n128	n129	n130	n131	n132	n133	n134
13	Output		n135	n136	n137	n138	n139	n140	n141	n142	n143	n144	n145	n146	n147	n148	n149	n150	n151
14	Rdson		n152	n153	n154	n155	n156	n157	n158	n159	n160	n161	n162	n163	n164	n165	n166	n167	n168
15	Breakdown		n169	n170	n171	n172	n173	n174	n175	n176	n177	n178	n179	n180	n181	n182	n183	n184	n185
16	Vbrdss		n186	n187	n188	n189	n190	n191	n192	n193	n194	n195	n196	n197	n198	n199	n200	n201	n202





Generating a Machine Learning Model

ML Regressions – Victory Analytics

MC based DoE design

- Linear random choice of sampling points for selected parameters
  - Epi_doping (1.5 … 2.5e16 cm^{-3})
  - Lap_um (7 … 13 µm)
  - Lgo_um (0 … 3 µm)
- Filter out "bad" datapoints
  - BV unphysically low close to Lgo=0

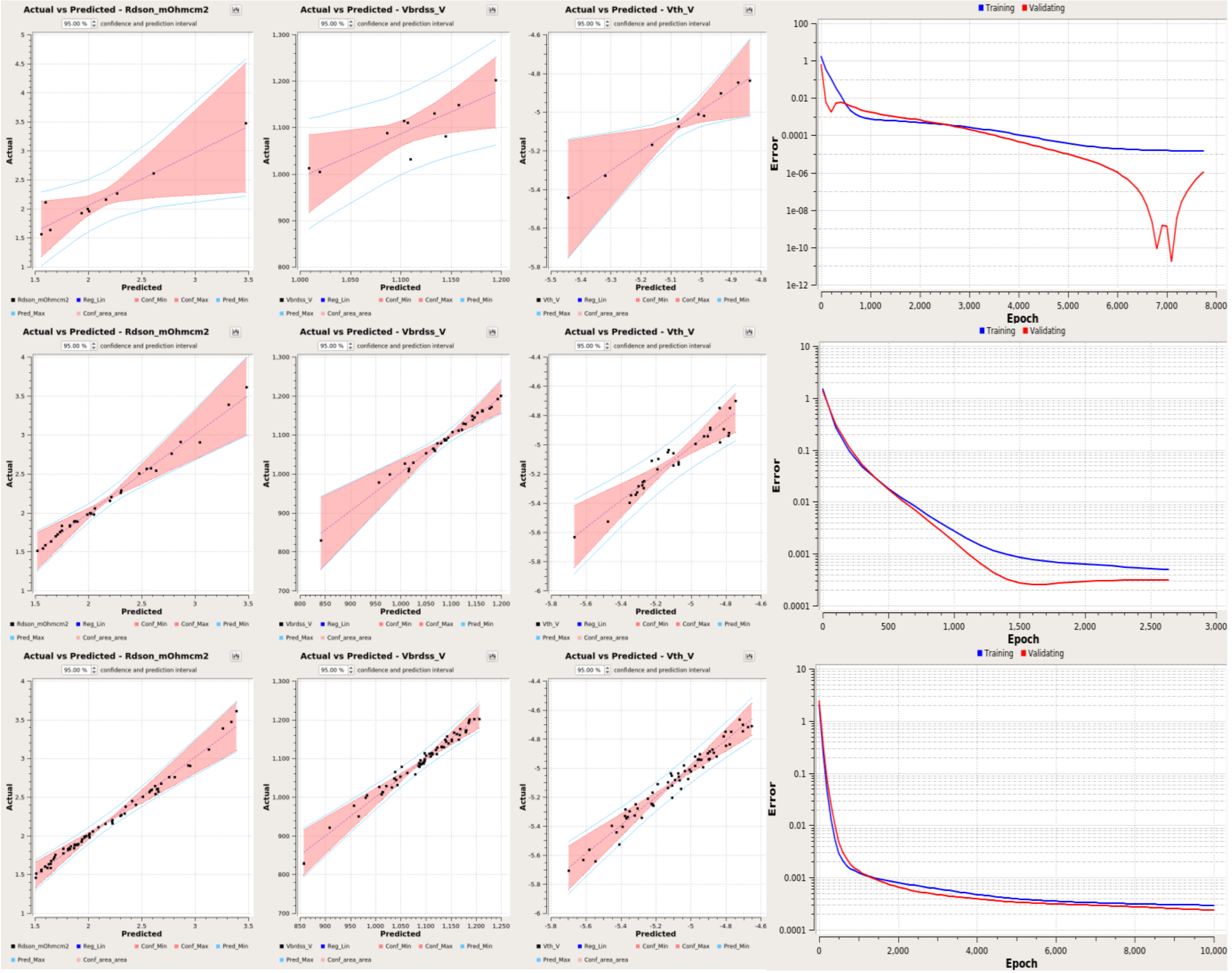
Generate ML regression model

- Use default settings in VA

Evaluate quality of model

- Tightness of "active vs. predicted" increases with number of sample points
- Loss curve takes L-shape

#	$R_{ds,on}$	$V_{br,dss}$	V_{th}
10			
32			
65			

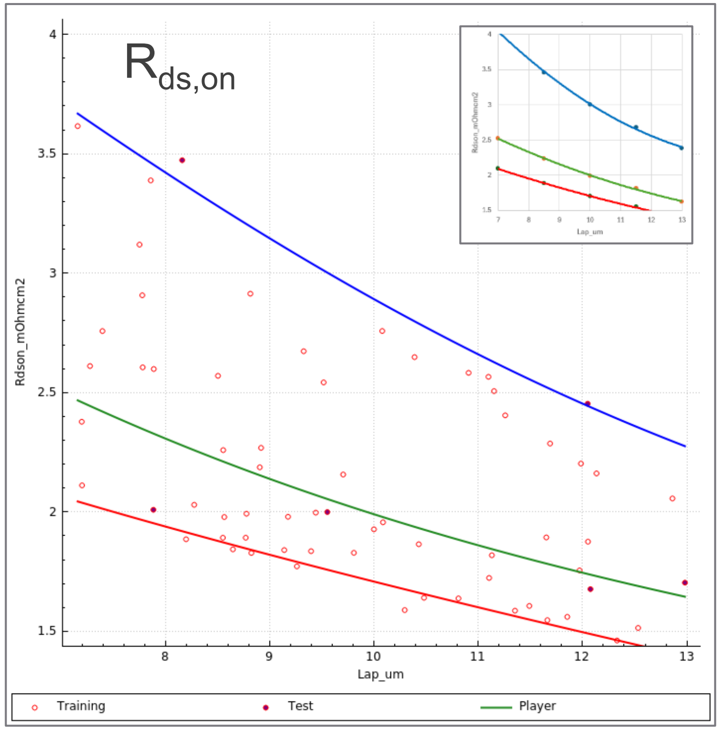


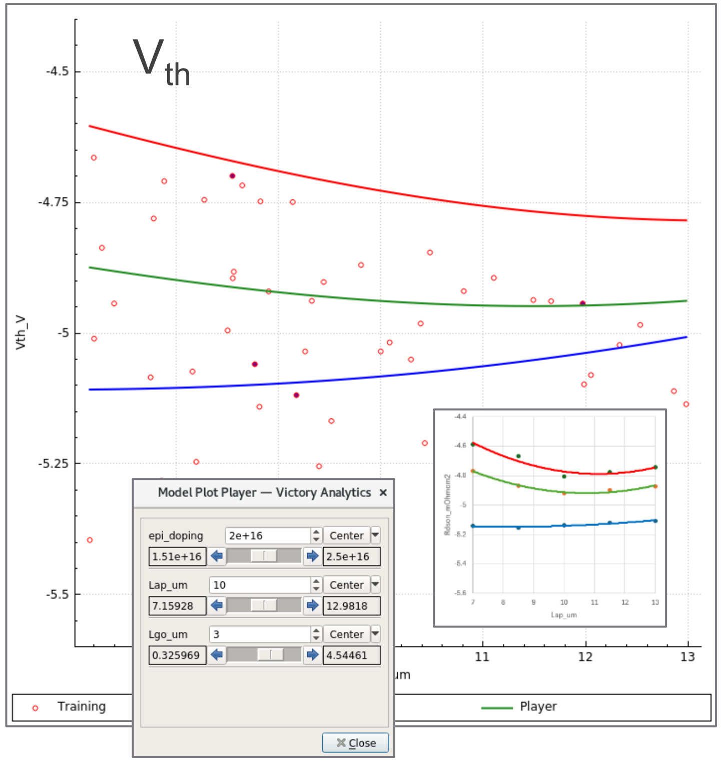
Inspecting Device FoM Trends

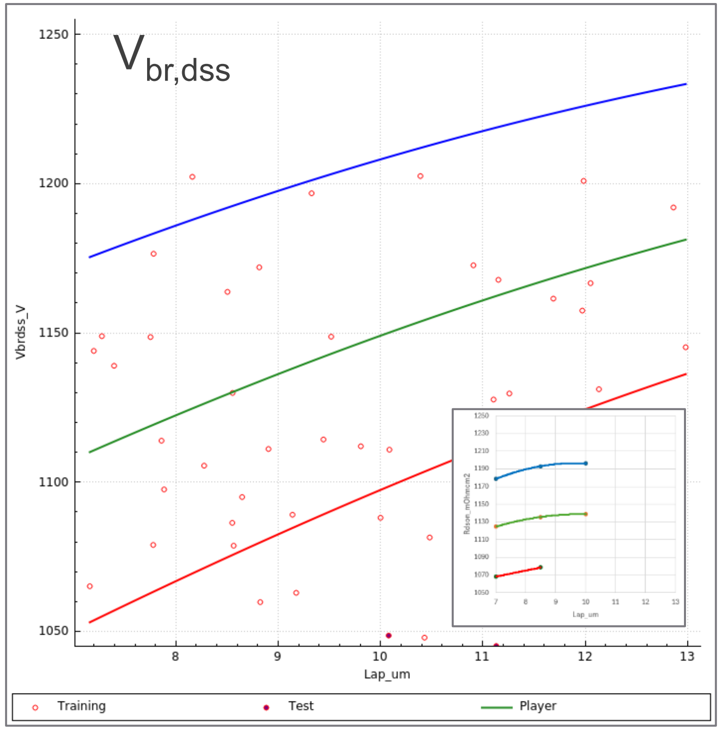
Model Plot Plus – Victory Analytics

Using the surrogate model to understand device trends

- FoM dependence on aperture (Lap_um) and epi-doping for a given gate-overlap (Lgo_um)







Note: the inserts show the same trends as extracted from the ML model but directly executing the TCAD deck. This is done to check the model accuracy.

Exploring Yield With Machine Learning (ML) Model

How Robust Is My Design To Lot-to-Lot Variation?

Engineer Objective

- Perform Process Capability Analysis
- Improve Robustness to Process Variation

Inputs to the ML Model

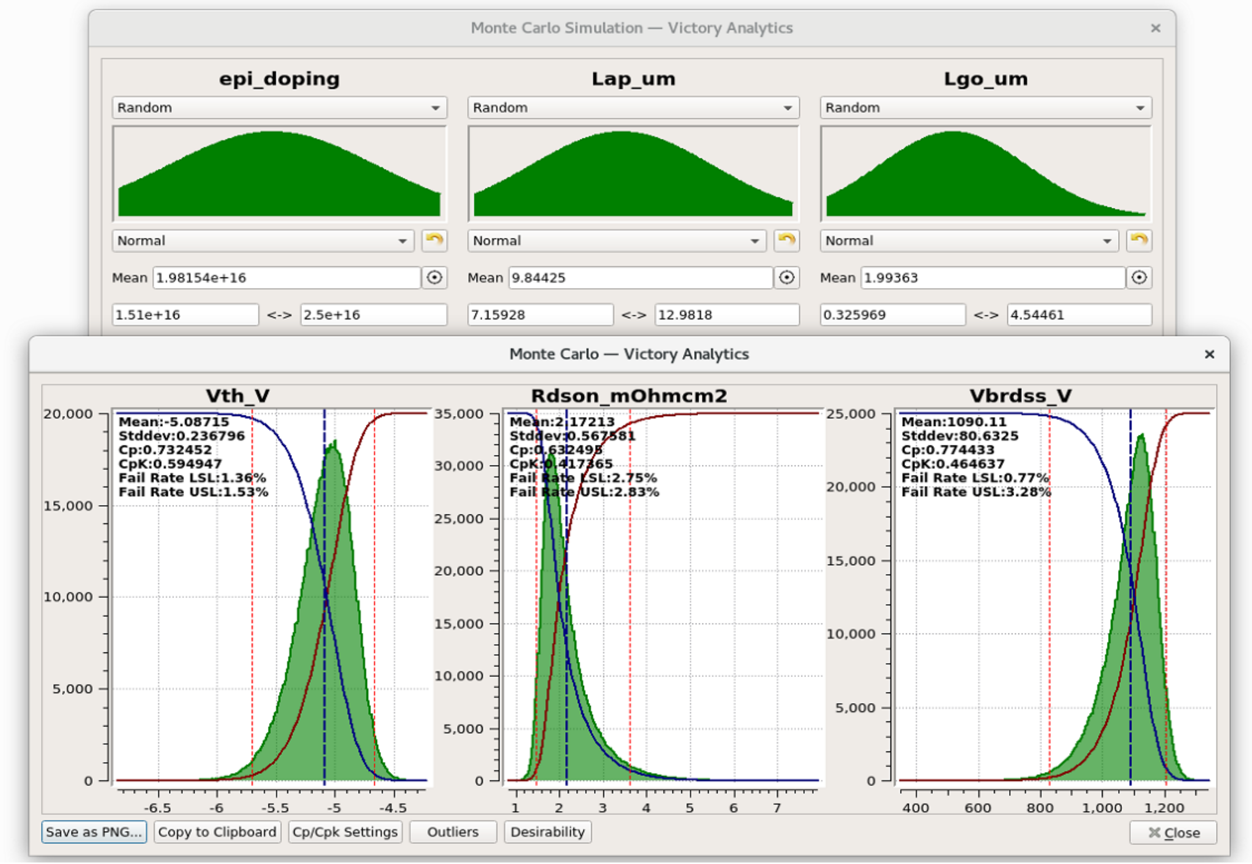
- Process Parameters:
  - Lot-to-lot variation in drift layer epi_doping.

Output from ML Model

- Process Metrics: epi_doping, Lap_um, Lgo_um
- Device Metrics: Vth, RdsOn, BV

Goals

- Perform **Monte Carlo Analysis**
- Cp/Cpk Analysis

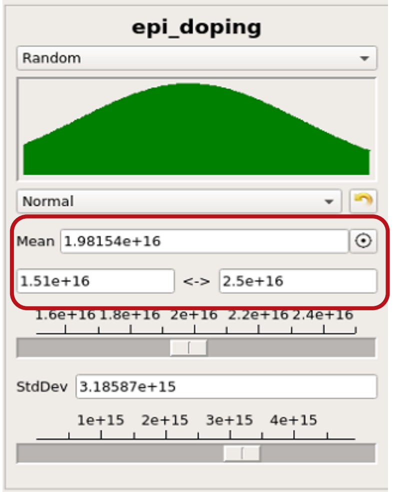


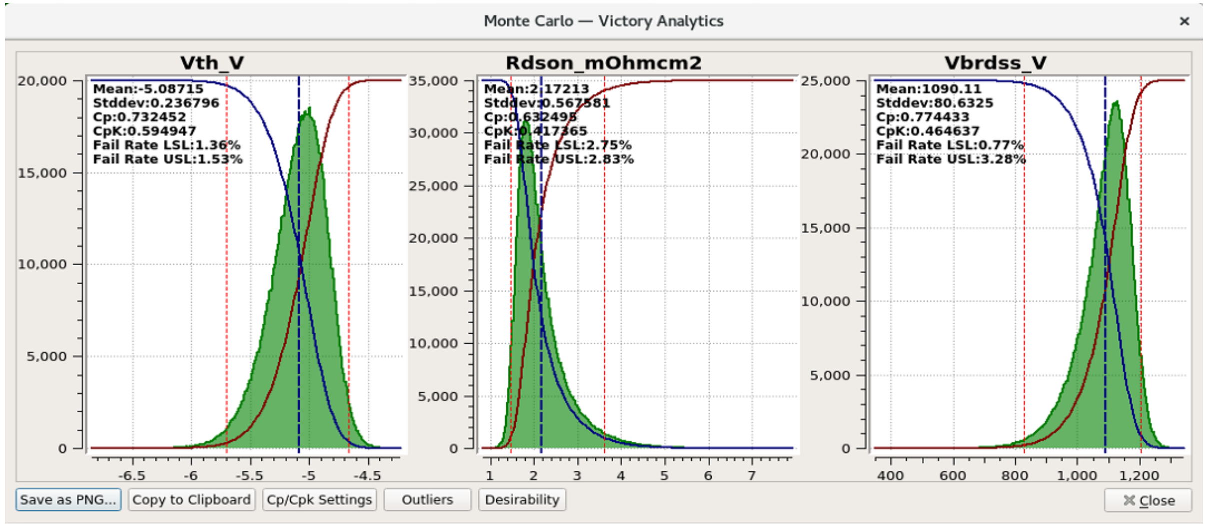
The ML model allows to analyze how process variation can affect yield.

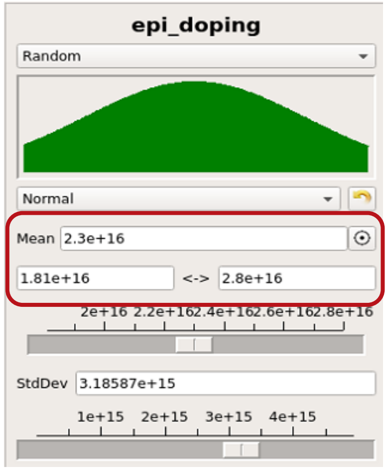
Exploring Yield With ML Model

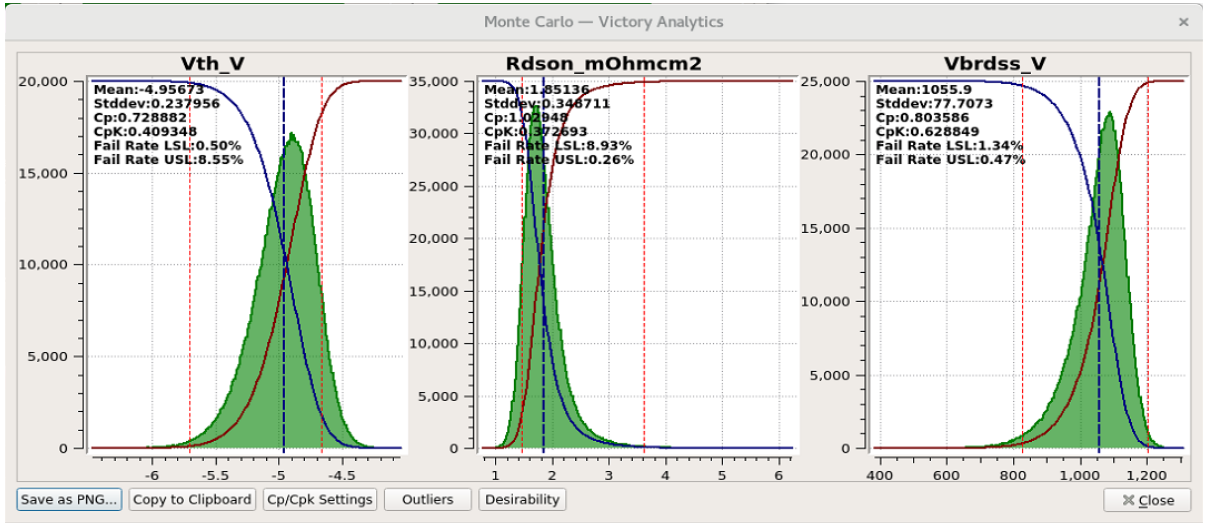
What-if scenarios

- ML model can be used to see the impact of shifting the nominal value of EPI doping process in the fab at a different location with the same distribution.





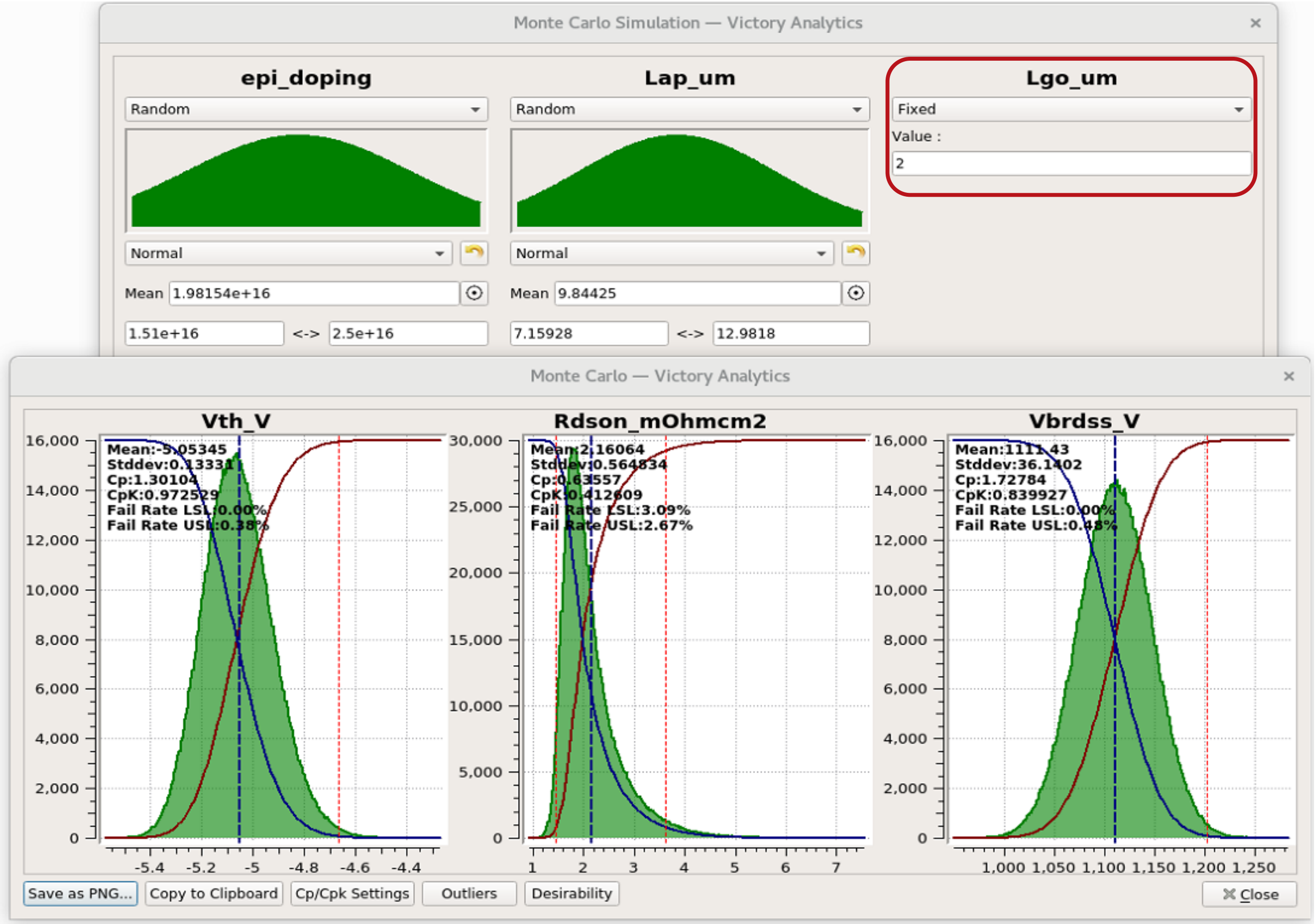


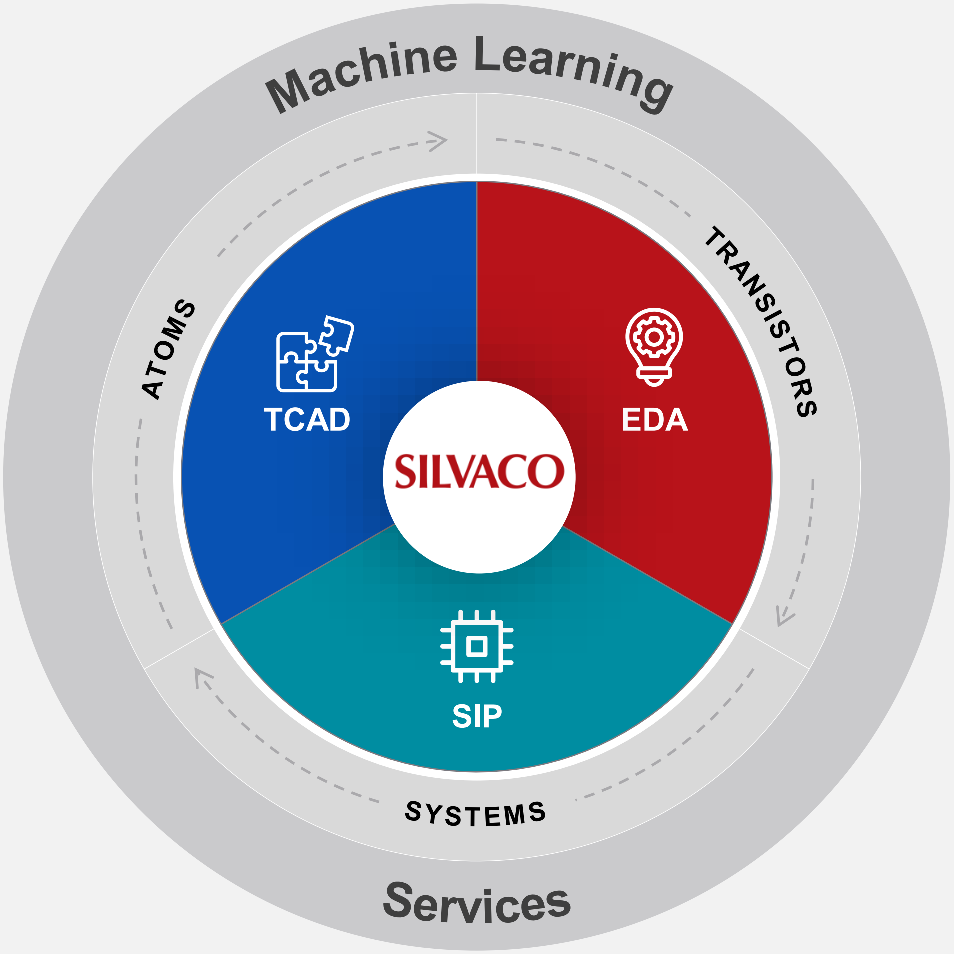


Exploring Yield With ML Model

What-if scenarios

- Fab Engineers could explore the impact on the FOMs (and yield) if feature control (gate overlap Lgo_um) is fixed. This may lead to a better capability being required (suggestion for new equipment) or a better understanding of the limitations impact on device performance.





Summary

- GaN Power Devices represent huge opportunities!
- TCAD is crucial to meet the challenges of design of GaN Devices
- Digital Twins enable optimization of manufacturing processes, reduced costs and increased yields
- Silvaco AI-generated Digital Twins/ML models are enabled by adding machine learning services on top of our core services
- Our tools enable the understanding of new technologies
- Our expertise spans from Atomistic to System-level IP
- Our solutions have been used in production flows for the past four decades
- Our agile R&D teams enable and adapt to your needs
- We are driven by your success

Thank you. | SILVACO

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