Fully Integrated GaN Solutions with Monolithic GaN-ICs

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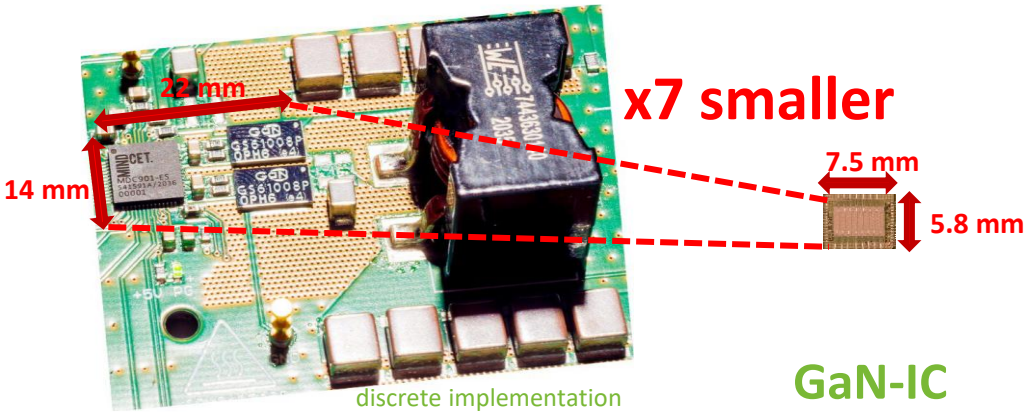
Bodo's Wide Bandgap Event 2025

Making WBG Designs Happen

The next wave of GaN is Integration and Intelligence[1]

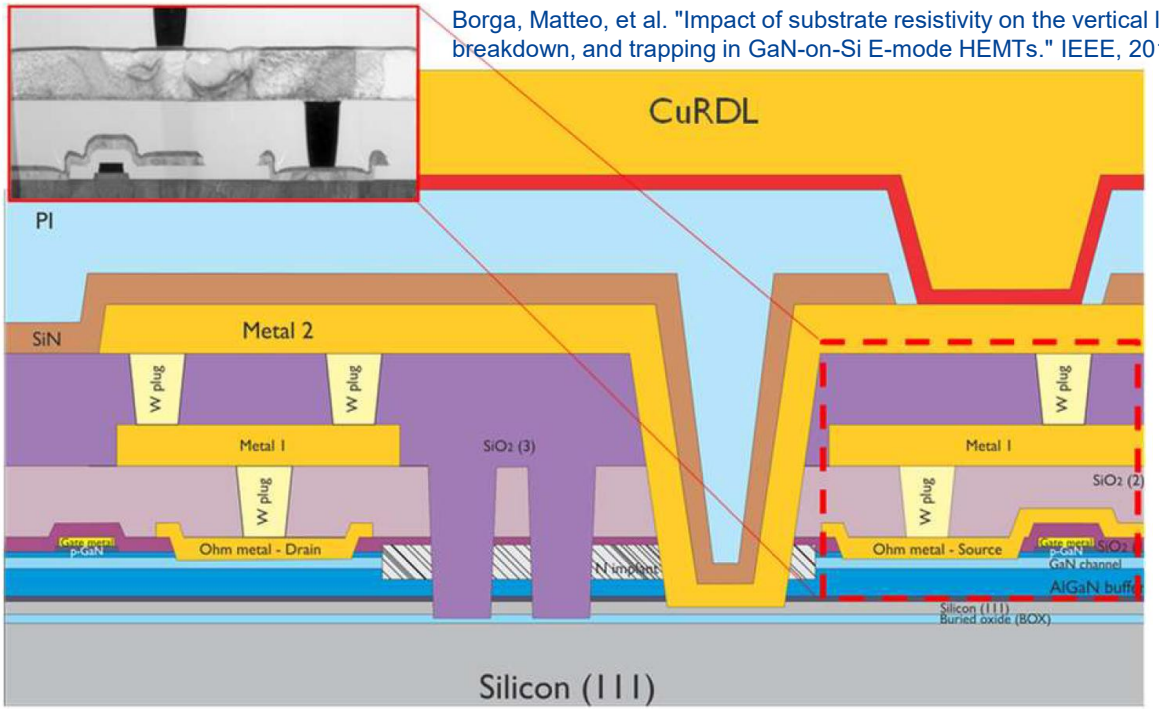


↑ Efficiency ↑ Power Density ↓ BOM ✓ Simplified Design

[1]The Future Prospects for GaN Technology (EPC, Oct 9 2025)

Boundry Conditions for GaN-IC

GaN-IC technology by IMEC: GaN-on-Si & GaN-on-SOI



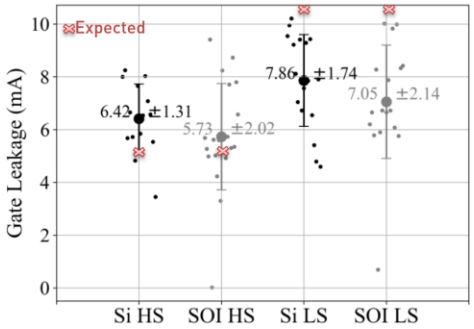
Borga, Matteo, et al. "Impact of substrate resistivity on the vertical leakage, breakdown, and trapping in GaN-on-Si E-mode HEMTs." IEEE, 2018

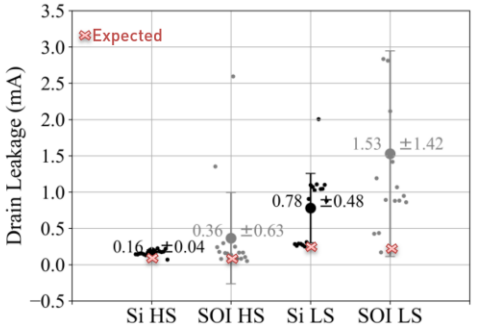
Boundary Conditions for GaN-IC

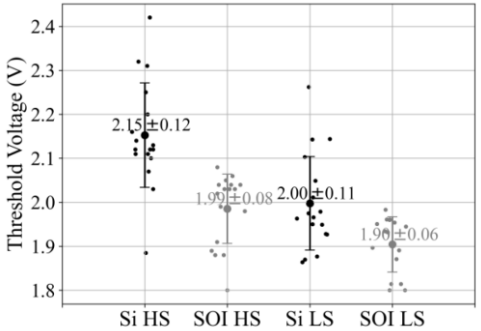
Technology based limitations

- **Higher leakage**

→ Limits quiescent current consumption







- **Low Vth matching** (x00mV-range)

→ Poses a challenge to circuit designers (delay matching, analog comparator levels, offset of analog amplifiers…)

Measurement results of HEMTs by using 17 samples from each type of transistor: 420 mm, 840 mm, GaN on Si or GaN on SOI.

Boundary Conditions for GaN-IC

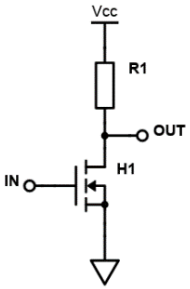
Technology based limitations

- **No complementary devices**

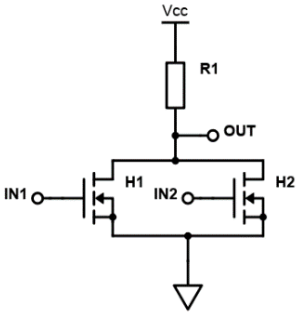
→ Puts a limit to complexity, increases power consumption (also static), asymmetric propagation, large on-chip area

- **No voltage reference (PTAT)**

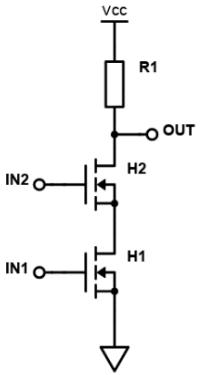
→ Requires off-chip voltage reference (e.g. Zener diode)



Inverter

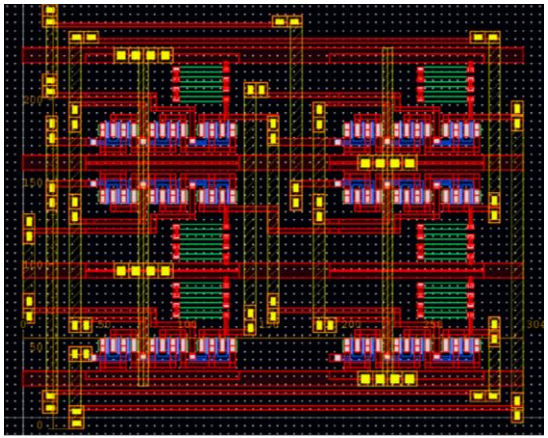


NOR



NAND

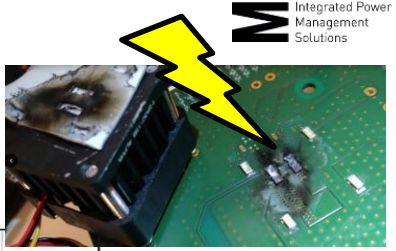
A GaN D-FlipFlop

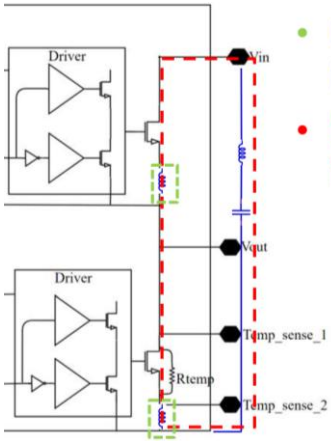


Boundary Conditions for GaN-IC

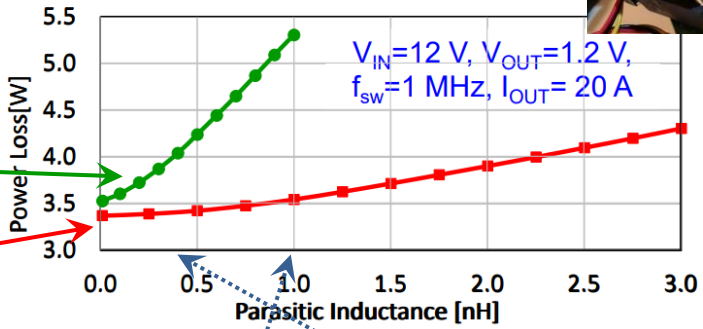
Subsystem integration considerations

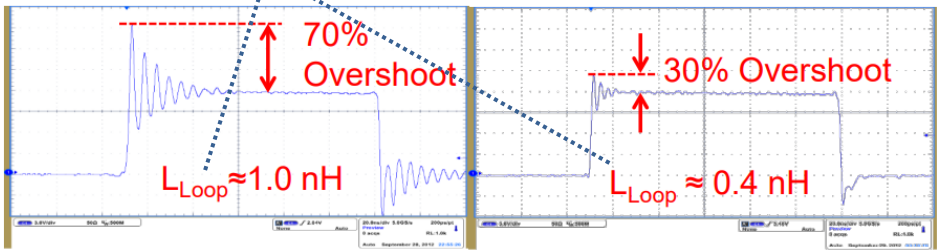
- GaN-IC still has parasitic inductance on source and DC-link
- Requires special care for packaging and PCB layout
- Ringing causes EMI and efficiency penalty and can cause breakdown





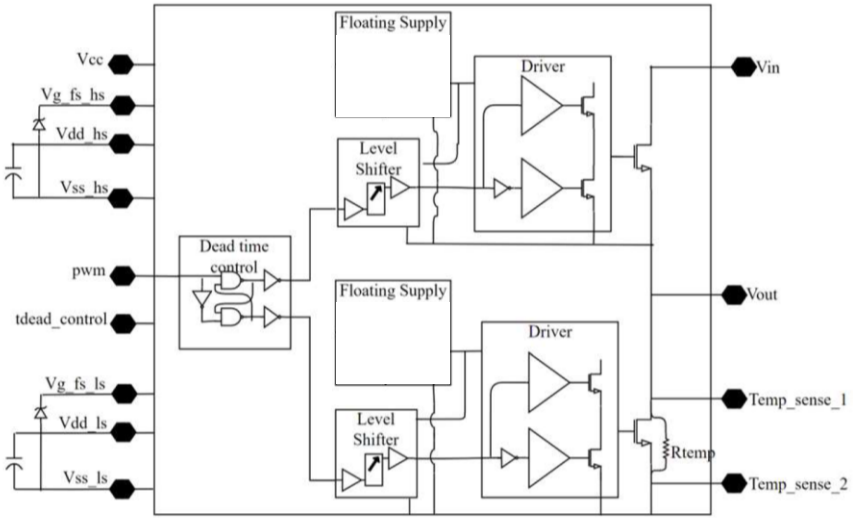
- Common source inductance
- Power loop inductance

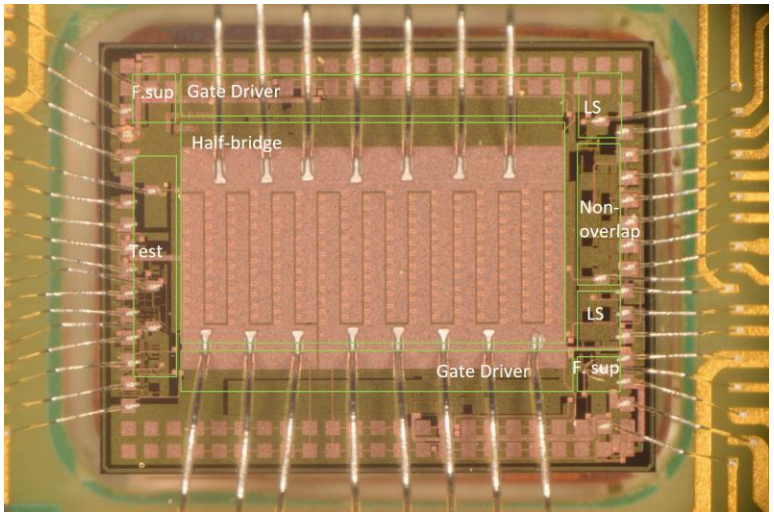




GaN-IC Half-bridge Implementations

40V Half-Bridge, IMEC GaN-on-Si





- LS = 1.4mOhm
- HS = 2.8mOhm
- Gate-drivers
- Level-shifters
- Floating supplies
- Bootstrap diodes
- Dead-time control
- Temperature sense (LS)

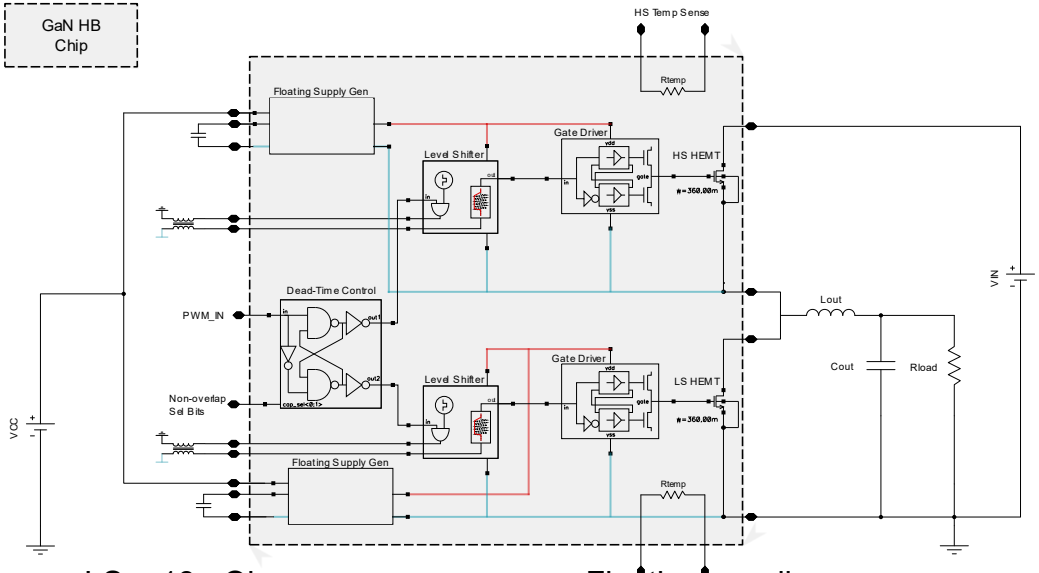
Die area = 40mm² (designed for flip-chip)

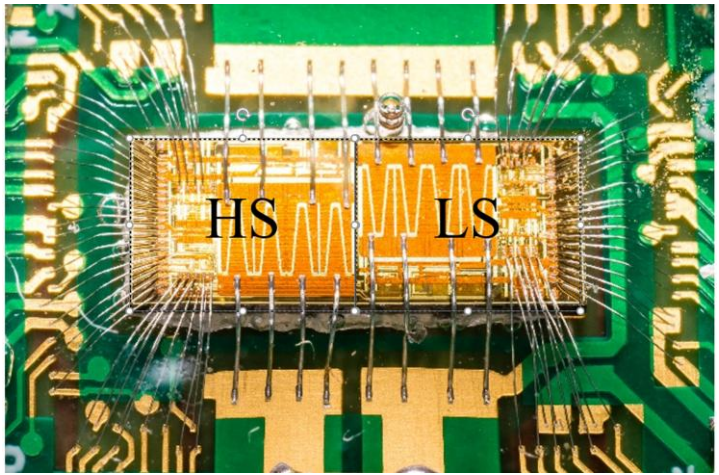
Application Target:

PoL DCDC e.g. 12V -> 1V @ 20A

GaN-IC Half-bridge Implementations

200V Half-Bridge, IMEC GaN-on-SOI





- LS = 18mOhm
- HS = 18mOhm
- Gate-drivers
- Isolated Level-shifters
- Floating supplies
- Bootstrap diodes
- Dead-time control
- Temperature sense (HS & LS)

Die area = 24mm² (Designed for flip-chip)

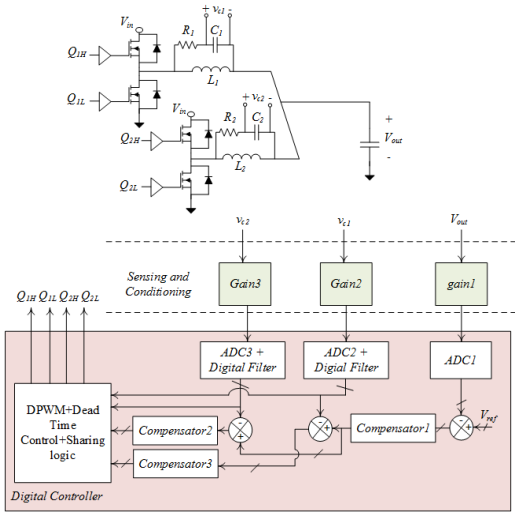
Application Example:

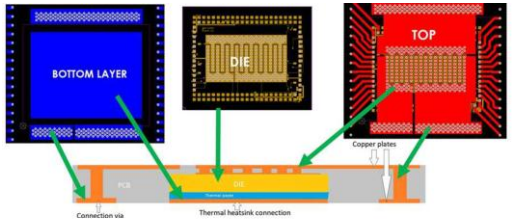
DCDC Converter e.g. 100V -> 12V @ 10A

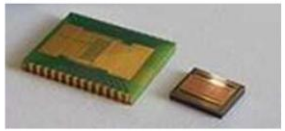
Measurements & Performance

40V GaN-IC

Digital Control for 2-phase PoL DCDC

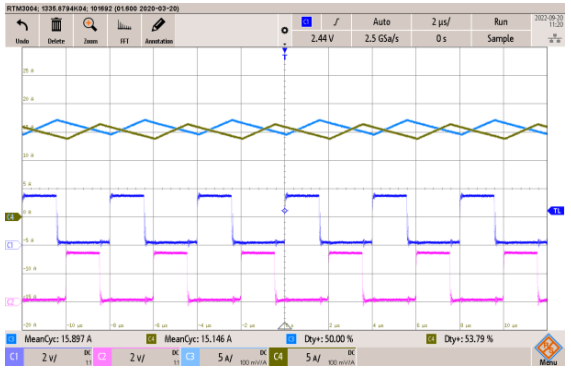


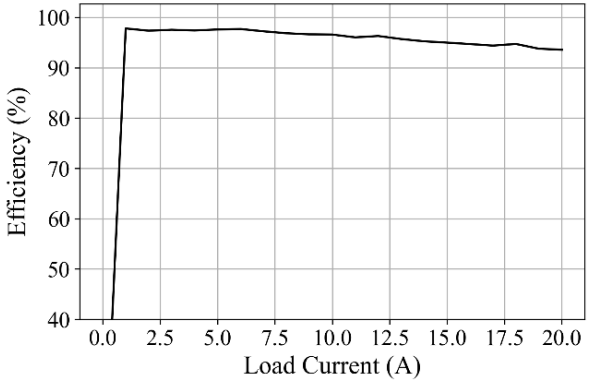




FR4 Embedded Package

Waveform (top) / Efficiency (bottom)



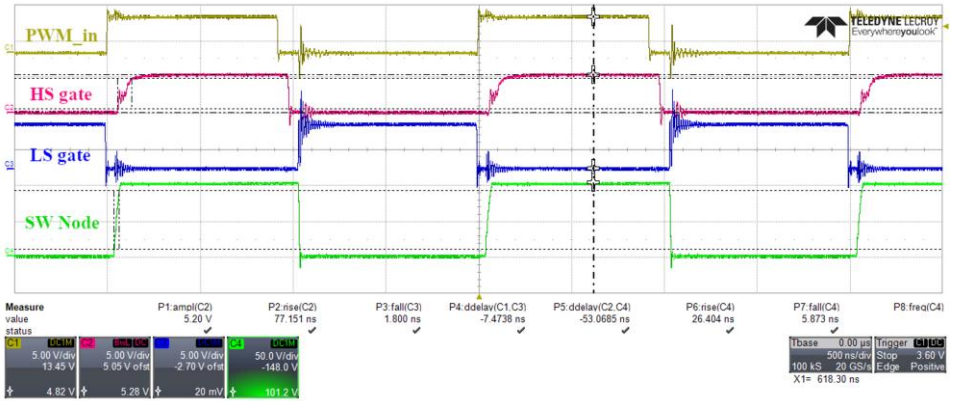


Measurements & Performance

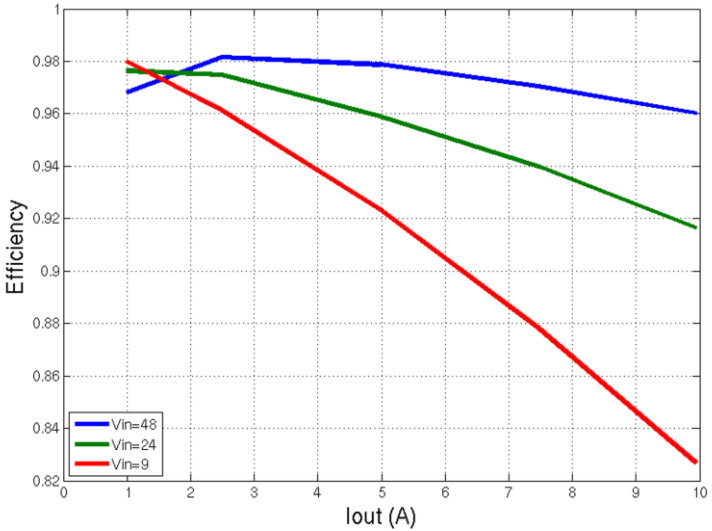
200V GaN-IC

FR4 Embedded Package

Waveforms



Efficiency @ 50% duty cycle



Future Outlook for GaN-IC

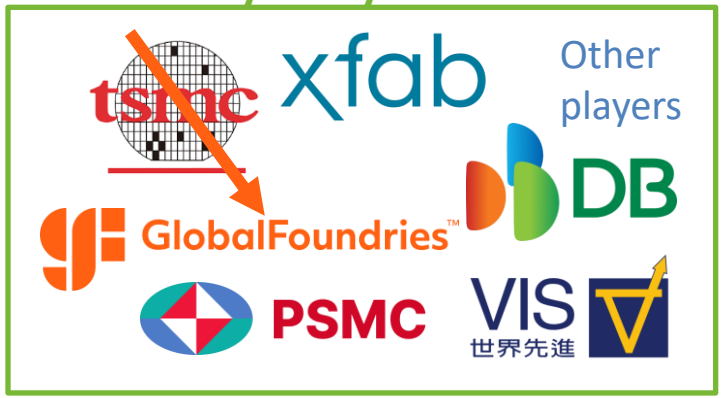
- Work on GaN technology side is ongoing to implement more devices:
  - MIM Capacitors -> more density than metal caps
  - High-ohmic resistors -> more stable than 2-deg resistors
  - Depletion GaN devices

- The **big breakthroughs** will be:
  - A **complementary GaN device** for analog and digital circuits (see history of “C”MOS)
  - A means of having a **PTAT voltage reference**

Conclusion

- GaN-IC is a commercial fact today: basic functionality enables “smart” GaN power stages
- Today there are fundamental GaN technology limitations → reliance on **silicon companion ICs** for more complex regulation, telemetry, control systems & protection requiring accuracy and speed
- GaN-IC technology is still relatively new and under constant development.
  - GaN market[2]: $355M (2024) → $3B (2030)
  - Established and new open foundries offering GaN processes
- The **GaN-IC revolution** will really kick in as limitations are overcome

GaN Foundry Ecosystem



[2]Power GaN 2025 report (prelim. results), Yole Group

Integration is the **future**.

The **future** is **GaN**.

Let's **Integrate** in **GaN** !

Acknowledgements

- ESA Project “GaNIC4S”
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Headquarters

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