Beyond the FET: Solving the Practical Challenges of SiC Gate Drive Design

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Allegro Microsystems

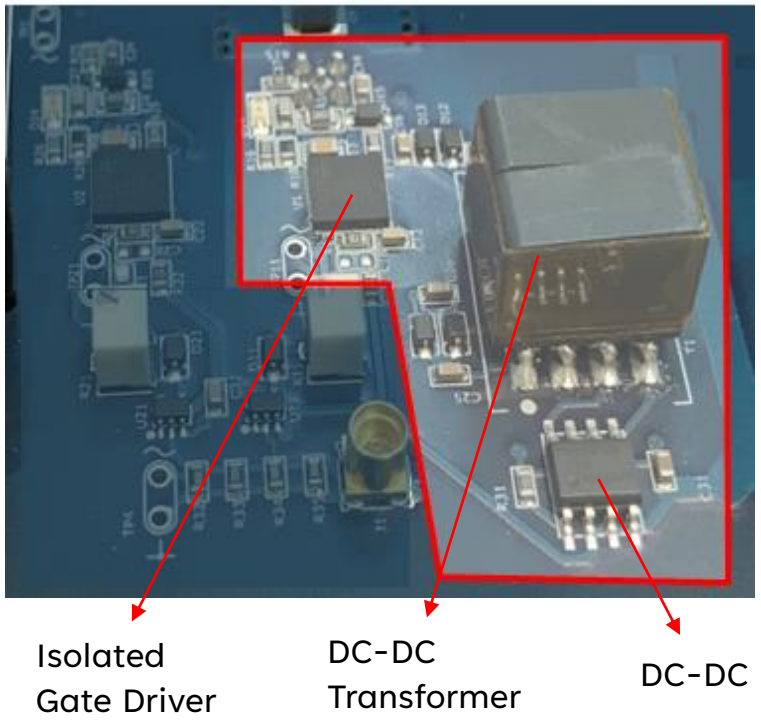
Bodo's Wide Bandgap Event 2025

Making WBG Designs Happen

SiC

Why Gate Drive Architecture Matters

- **Gate Drive Architecture Defines SiC System Performance and Board Size**
  - Bias generation is major contributor to PCB size
  - Bias generation increases complexity and Time-2-Market
  - High dv/dt stresses the entire system
  - EMI constraints limit switching speeds



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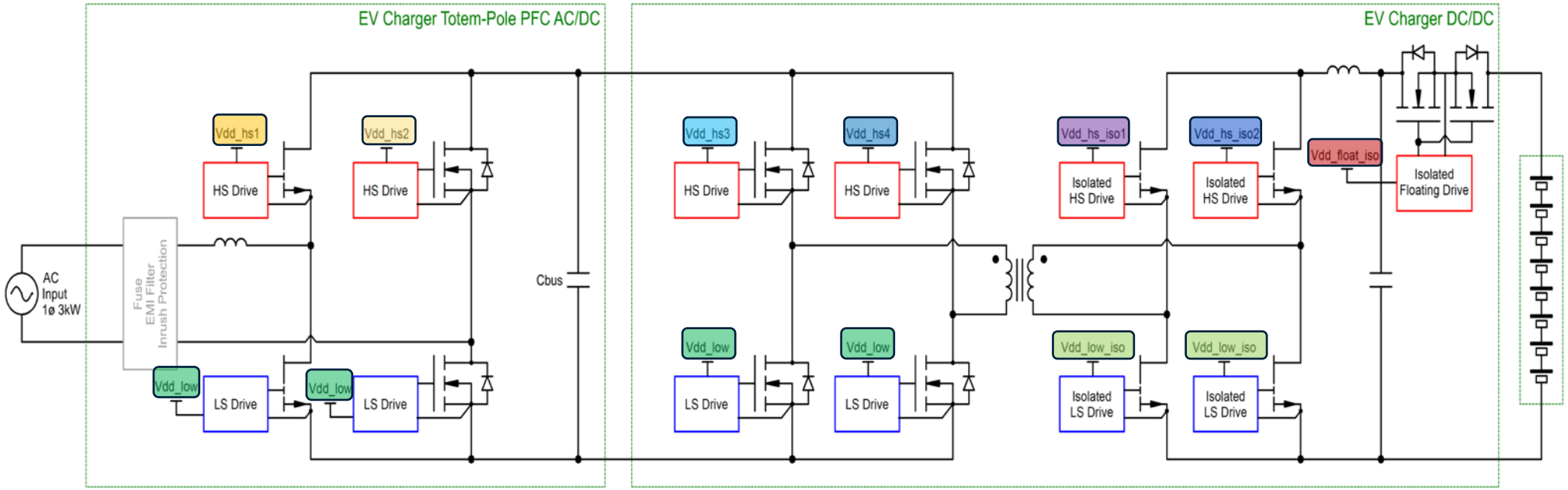
Conventional Bias Generation: Complex and Bulky

Gate-Drive Bias Increases System Cost and Size

- Multiple isolated supplies
- Larger PCB footprint
- More coupling paths → more EMI
- Higher qualification effort

Power Rails
Vdd_low
Vdd_hs1/2/3/4
Vdd_low_iso
Vdd_hs_iso1/2
Vdd_float_iso



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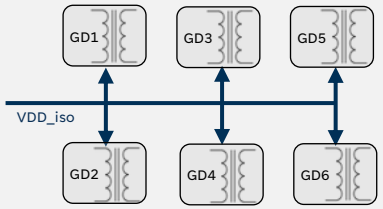
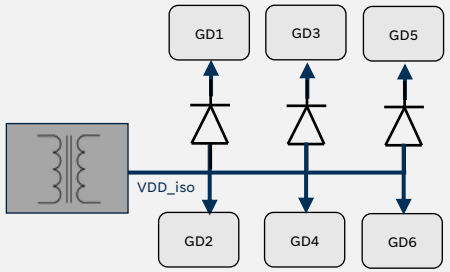
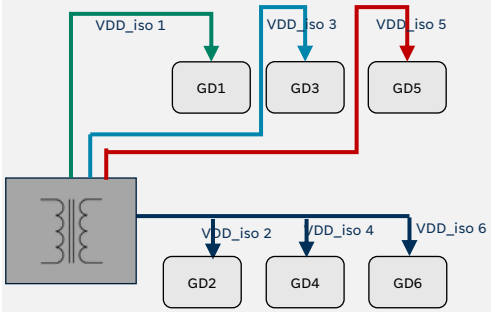
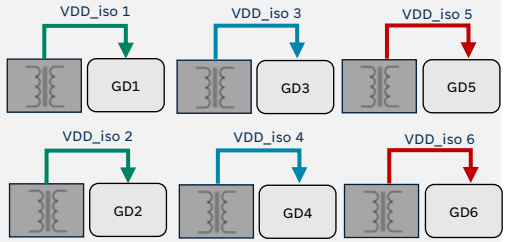
Introducing Power-Thru™

Power-Thru fundamentally simplifies the architecture
Instead of generating isolated bias rails off to the side, each gate driver generates its own rails locally.

	Allegro Power-Thru	Centralized	Semi-distributed	Distributed
				
Description	Micro DC-DC built-in each driver	Single Vdd_iso + bootstrap	Single transformer w/ 6 Vdd_iso rails	6 independent transformers
Power Density	High	High	Low	Low
Complexity	Low	Low	Moderate	High
Efficiency	Moderate	Moderate	Moderate	Moderate
Robustness[1]	High	Low	Moderate	High
Cost	Moderate	Low	Moderate	High
Reliability[2]	High	Low	Moderate	High

1. Robustness = ability of system to keep functioning if a key component fails
2. Reliability = single point of failure

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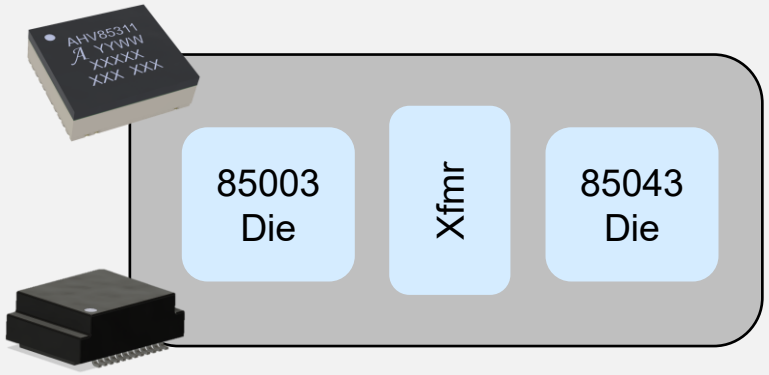
Two Implementation Paths

Power-Thru™ is Available in Two Forms

1. AHV85311 Module – fast, easy integration
2. AHV85003/043 Chipset Combo - flexible, cost-optimized

AHV85311



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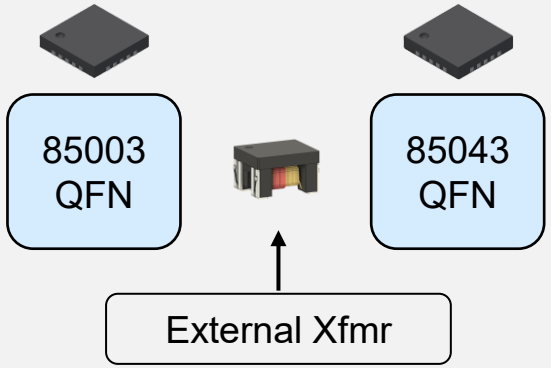
AHV85003 & AHV85043



Module Solution

- 2 package options (leadless and leaded)
- 13.2 x 11.5 = 151.8mm²; 16.9 x 10.3 = 174.1mm²

Chipset

- External transformer required
- 2pcs QFN4x4 (32mm²)

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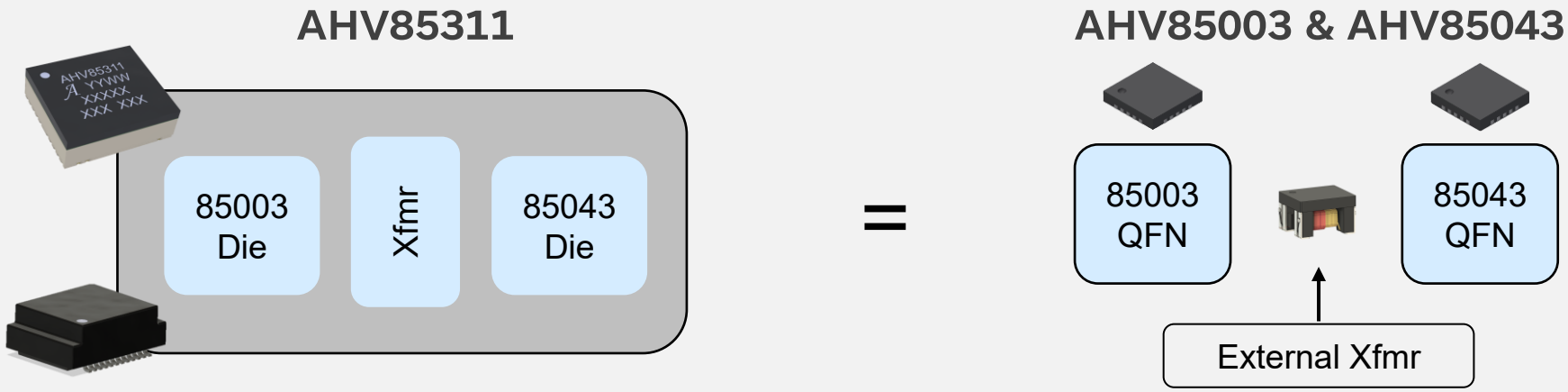
RTM in Dec 2025: AHV85003 & AHV85043 as a cost-optimized alternative



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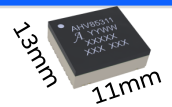
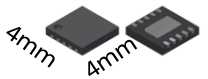
- 2pcs QFN4x4 (32mm²)

	AHV85311-NK	AHV85311-NL	AHV85003 & AHV85043
			
Integrated Transformer	✓	✓	✗
Isolation level	Reinforced 5kV	Reinforced 5kV	depends on selected transformer
Release to Market (RTM)	July 2026	October 2026	**December 2025**

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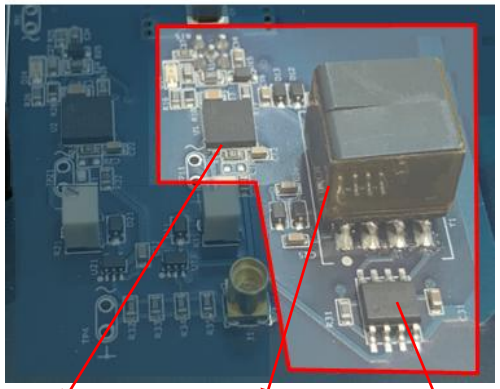
ALLEGRO'S FIRST **POWER-THRU SIC GATE DRIVER:**
1 DRIVER, 3 VERSIONS

Integrated bias supply



Isolated Gate Driver

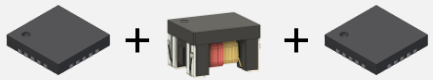
DC-DC Transformer

DC-DC

Available in 3 versions.

1.

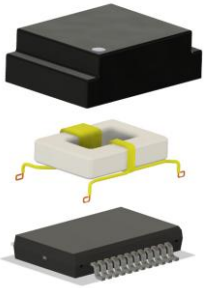
RTM: Dec 2025



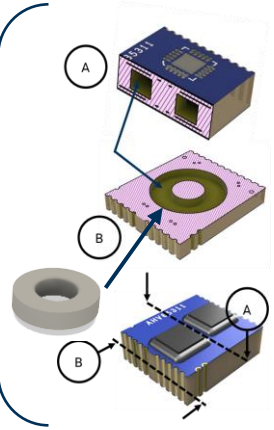
QFN prim + ext. xfmr + QFN sec chip chip

2.

3.



NL: Isolated Gate Driver + DC-DC + Transformer

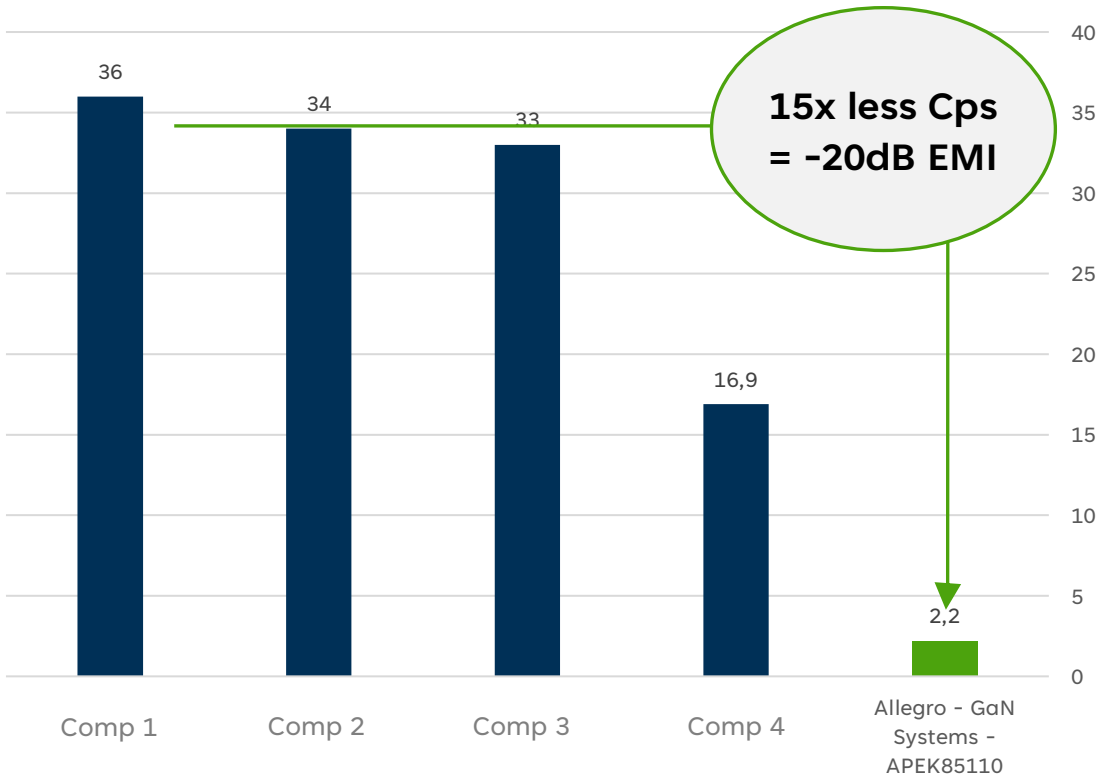


NK: Isolated Gate Driver + DC-DC + Transformer

- **Cost reduction through reduced BOM**
- **Faster T2M**
- **PCB Space Reduction**
- **Higher Efficiency with Power-Thru**

BEST-IN-CLASS EMC PERFORMANCE

Lowest Common-Mode Capacitance



- Minimize EMI
- Reduce Switching Losses
- Enable High-Frequencies

BEING FLEXIBLE MINIMIZING REDESIGN EFFORTS

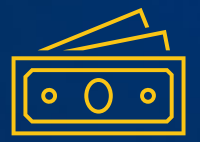
Enabling Multi-Source SiC Strategy

- **AHV85311 / AHV85003 + AHV85043:** variably orderable in 15V / 18V / 20V turn-on V_{SECP} and adjustable on turn-off V_{SECN} between 0V and -5V
- Enabling dual source approach with e.g., these vendors:

life.augmented onsemi ROHM SEMICONDUCTOR

Wolfspeed nexperia Infineon

Reduce Dependency, increase Supply Resilience



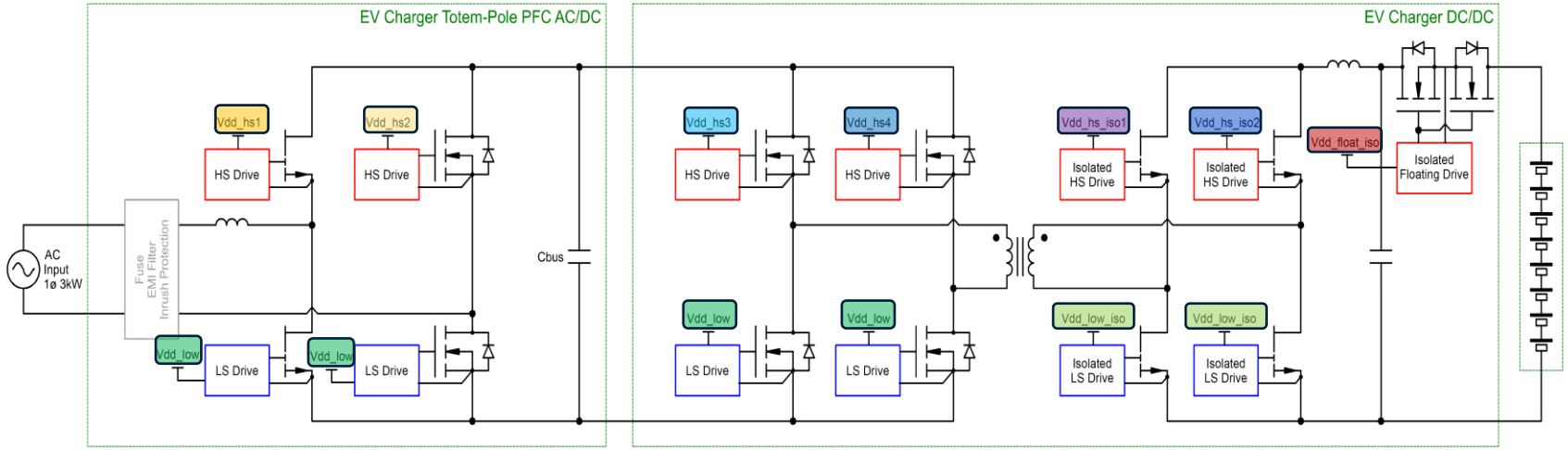
Cost Flexibility

Regionalize BOM

Benefits applied to PFC / DCDC

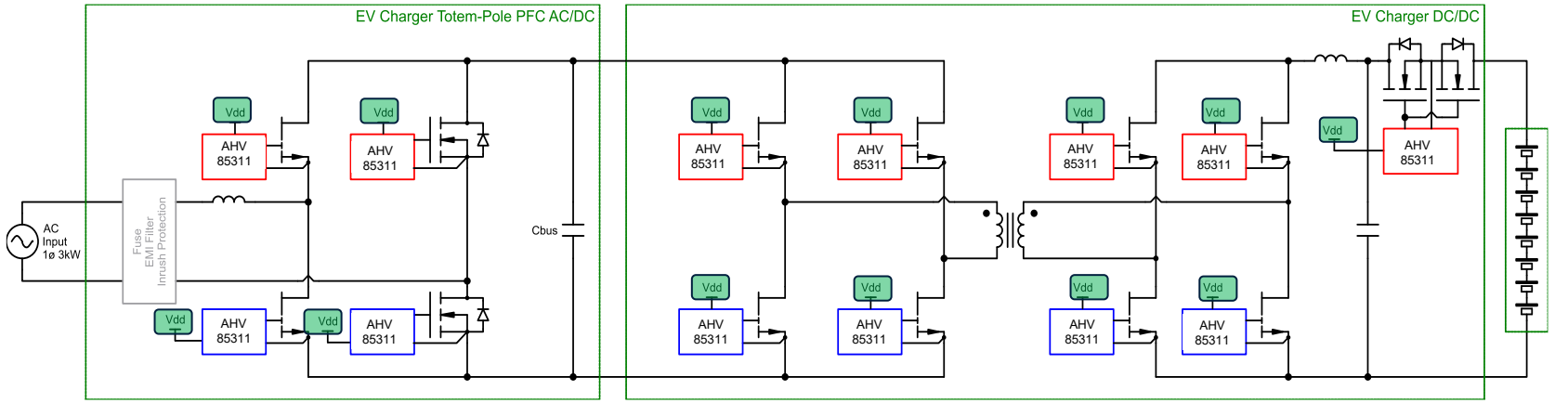
Power Rails
Vdd_low
Vdd_hs1/2/3/4
Vdd_low_iso
Vdd_hs_iso1/2
Vdd_float_iso

Conventional bias generation – complex and bulky



Simplified Topology with Power-Thru!

- Reduced BOM
- Better EMI behavior
- High isolation robustness
- Faster design cycles



Power Rail
Vdd_low

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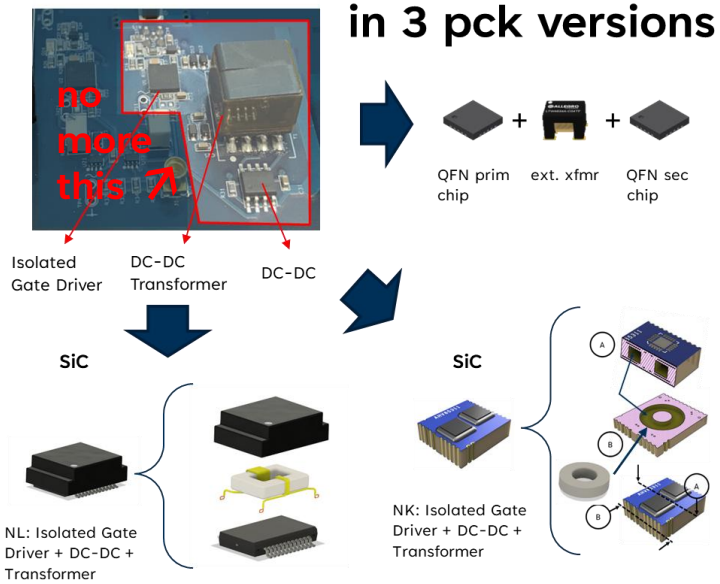
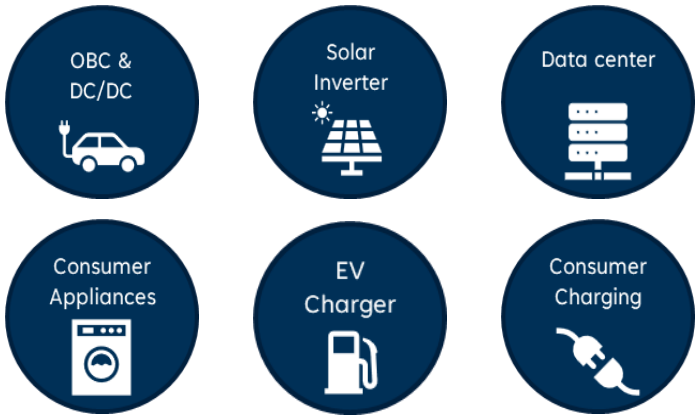
Allegro‘s first SiC Gate Driver AHV85311 – Order Samples Now!

Integrated BIAS Supply in 3 pck versions

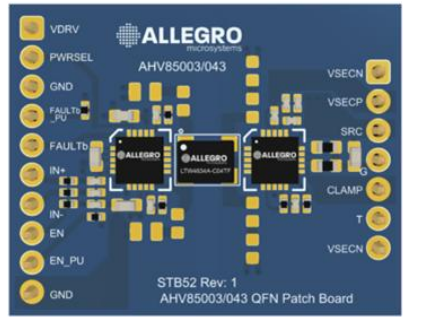




Elevate your SiC Designs!

- **Final Samples available**
- **QFN chipset RTM** in Dec 2025
- **Be flexible on your SiC** w/ V_{SECP} = 15V, 18V, 20V

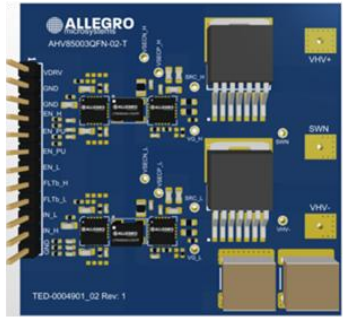
Daughter test cards



APEK85003K15ES-02-MH

APEK85003K18ES-02-MH

Half-bridge eval boards



APEK85003K15ES-04-MH / Wolfspeed

APEK85003K18ES-04-MH / Onsemi

Best-in-Class EMI: **-20dB**

	AHV85311NK	AHV85311NL	AHV85003 & AHV85043
	NK 13.2mm 11.5mm	NL 10.3mm 16.9mm	QFN 4mm 4mm
Integrated Transformer	✓	✓	✗
Isolation level	Reinforced 5kV	Reinforced 5kV	depends on selected transformer
Release to Market (RTM)	July 2026	October 2026	December 2025

QFN chipset as cost optimized alternative

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Elevate Your SiC Design with Power-Thru™

Thank you.

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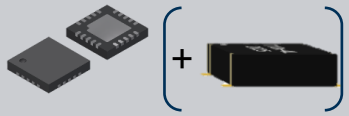
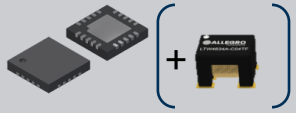
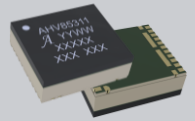
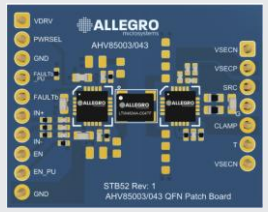
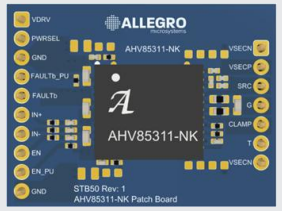
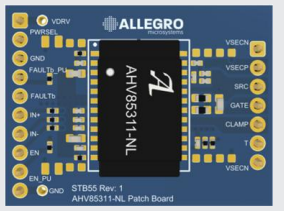
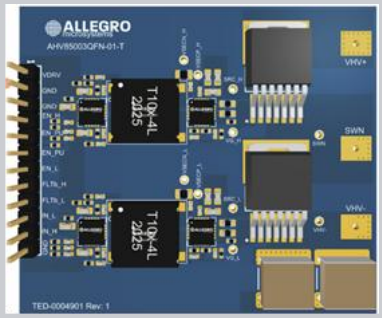
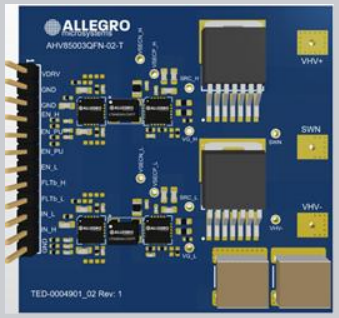
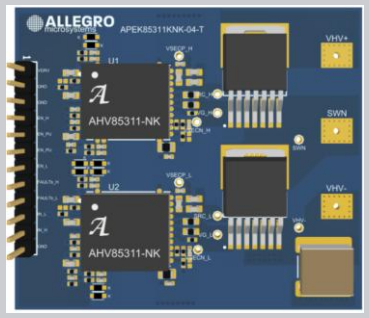
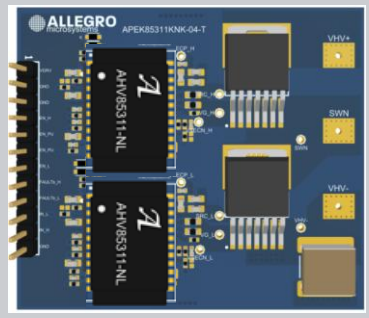
Fall 2025 Samples & Boards for your SiC Designs

	QFN				NK		NL	
	Reinforced isolation		Functional / Basic isolation					
	Schematic	Scheduled	Schematic	Scheduled	Schematic	Scheduled	Schematic	Scheduled
Samples		available		available		available		Jan 15th
Daughter Test Cards		available		available		available		January
Half-Bridge Eval Boards		available		available		available		January

Please specify your desired drive voltage: 15V, 18V, (20V available from 01/26) and for QFN board requests the isolation type

External transformers for discrete QFN Chipset Combo sampling need to be bought from transformer vendors – we can recommend PNs or provide spec

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QFN CHIPSET COMBOS ARE READY TO USE NOW

Various Transformers are being qualified - Collaterals are available

- We are qualifying transformers from premium suppliers and experienced low-cost alternatives
- Eval boards are available today
- Collaterals like STEP files, Altium schematics, User guides are ready to be used