Assessing the aggregate behavior of paralleled SiC Mosfets

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Bodo's Wide Bandgap Event 2025

Making WBG Designs Happen

SiC

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A leading measurement insight company committed to performance and compelled by possibilities. Tektronix designs and manufactures test and measurement solutions to break through the walls of complexity and accelerate global innovation.

Tektronix®

High-fidelity measurements, analysis and generation of high-speed signals with best-in-class **oscilloscopes**, **probes**, signal **sources**, **RF** measurement instruments, **software** and **services**.

- High signal frequencies up to 70 GHz
- Isolated Probing with Dynamic range up to +/-2.5KV
- Medium-range AC and DC measurements
- Voltage: mV's to kV
- Current: mA to 100's of amps

78-year history

KEITHLEY
A Tektronix Company

Precision instruments and systems for sourcing and measurement of analog voltage and currents suitable for **characterizing and validating power semiconductor devices**.

- Extremely precise DC measurements
  - Voltage: nV to kV
  - Current: fA to 10's of amps
- Medium-range DC power output in 10's or 100's of W

78-year history

Elektro-Automatik

High-power efficient DC power supplies, **bidirectional** supplies, and **electronic loads** critical for development, test, simulation, and commercialization of products for tomorrow's electrified industries

- DC power outputs up to 3.84 MW
- DC voltage outputs up to 2000V
- DC Current outputs up to 64000A
- Regenerative loads return power to the grid at > 96% efficiency

50-year history

Paralleled Mosfets Topologies

WHY AND WHERE

Need:

- Meet Increasing Power Demand -> Increase Current Capability
- Individual Current Rating is limited
- Dissipation capability is limited
- **-> Mosfets Paralleling**

Applications:

- Solid-state switching in Power Distribution
- High Power DC-DC Converters, PFCs (AC/DC)
- Motor Drives and Inverters
- Protection Circuits in Battery Management
- Audio Amplifiers
- Induction Heating

Paralleling Advantages of SiC MOSFETs Over IGBTs

- SiC MOSFETs often have a higher $R_{DS(ON)}$ temperature coefficient than Si IGBT V_{CE} characteristics, which acts as a balancing mechanism when temperature imbalances exist
- SiC MOSFETs are more thermally conductive, allowing for better device-level heat dissipation and stable operating temperatures
- IGBTs have a steeper transconductance curve such that small changes in gate voltage near threshold have a larger effect on conduction as compared to SiC MOSFETs

Current Sharing Challenges

NOT A STRAIGHT FORWARD SOLUTION

Theoretically it is necessary to :

- Ensure **balanced** static and dynamic currents
- Ensure **even** conduction and Switching Losses and **Stresses**

Time consuming phase in:

- Precise simulation model and simulating condition environment
- Performing Validation with Test Equipment hardware and application software

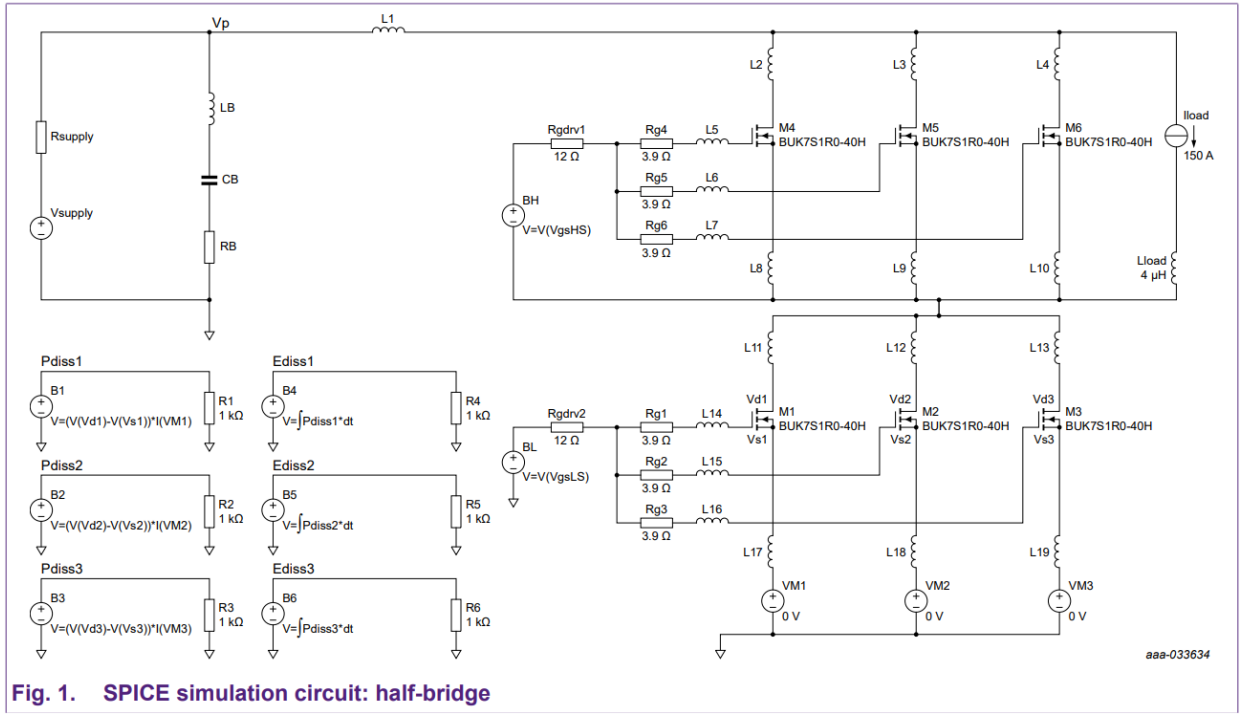


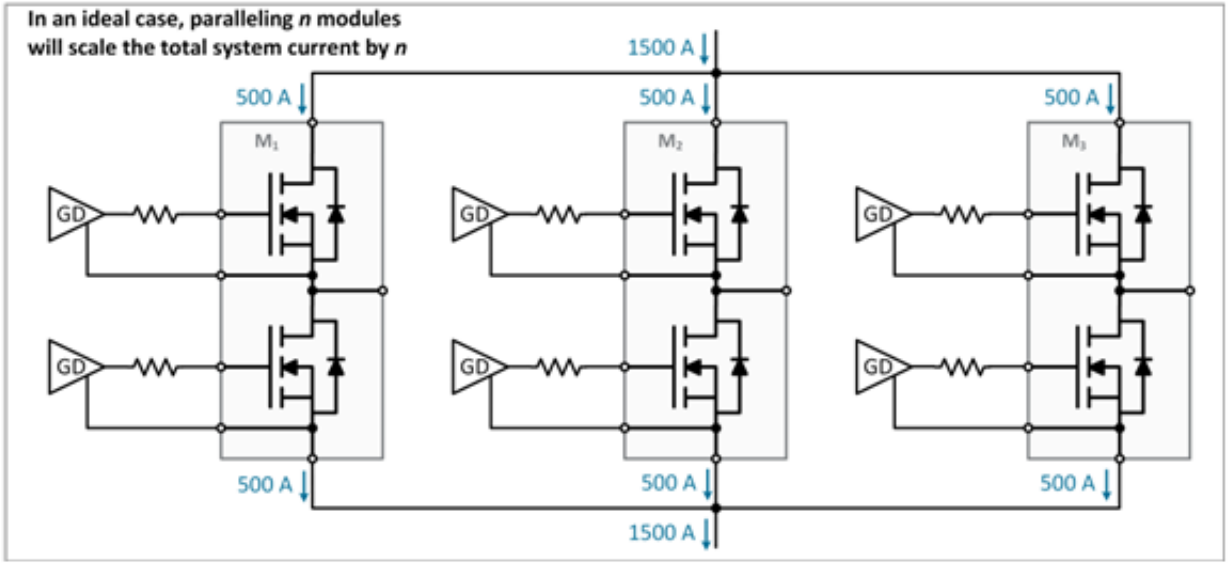
Fig. 1. SPICE simulation circuit: half-bridge

From Nexperia App Note: AN50005 Paralleling power MOSFETs in high power applications

Paralleling is Not Perfect

Ideal current sharing in the modules depends on various factors like:

- System layout- Parasitic inductance of commutation loop and gate loop, impedance of the load
- Gate driver configurations- Driving speed, timing delays can lead to circulating currents
- Module parameter mismatch- On-state resistance ($R_{ds(on)}$) and threshold voltage (V_{th})
- Heatsink configuration- Temperature imbalance can cause current imbalance



Rds ON

Static:

- Power Mosfets Static Rds ON has **positive** Temperature Coefficient

Dynamic:

- Switching Over Stress **->** Premature Failure

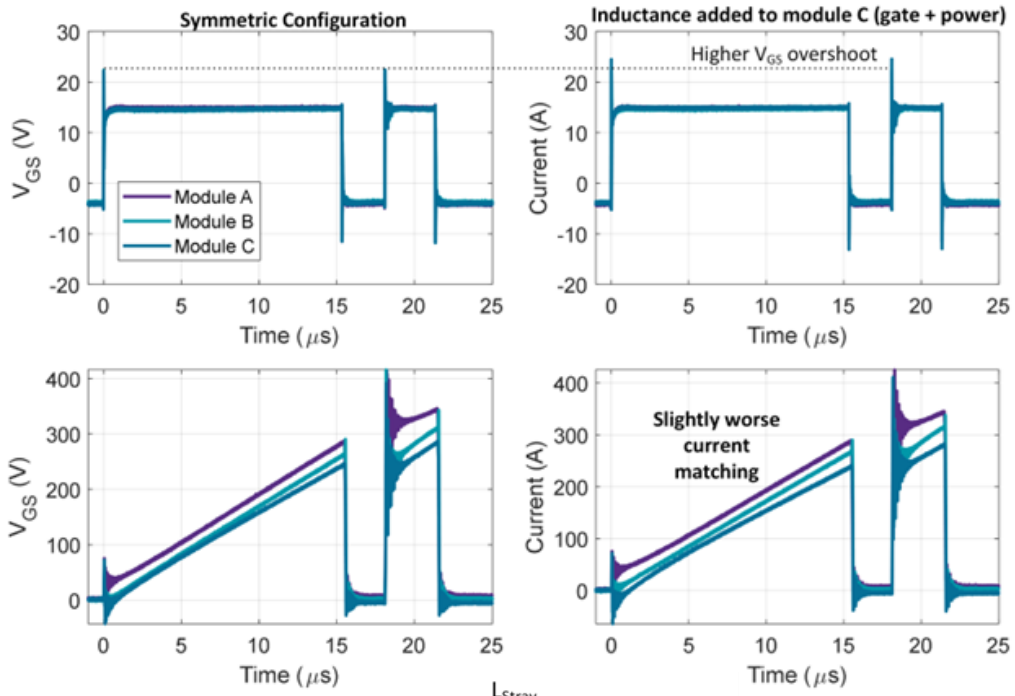
- Plotting Rds ON and TJ and impact on Id over Time

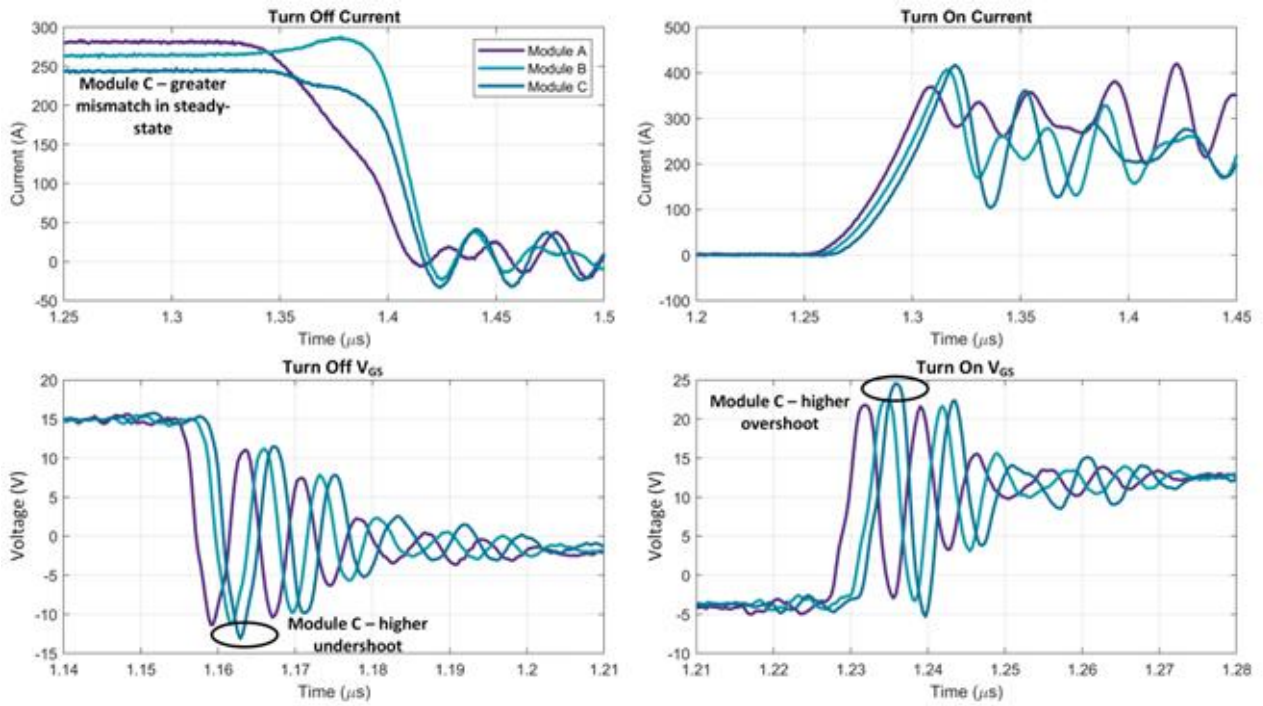
- Transfer characteristics and transconductance matching!

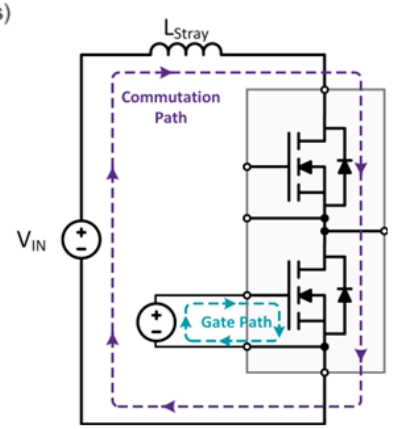
Strategies for Implementation according to Design Books

- **Ultra symmetric layout. Match traces parasitic in simulation.**
- Recogize linear orientation of switches and path.
- Easier for low voltage (gate driver), less easy for HV path
- **Active Gate Control (gate voltage adjustment). Improves EMI**
- Cons: Require current feedback, increases losses
- **Inductance insertion in commutation path**
- Cons: gate-source currents, voltage ringing, damages
- Need of shunts in series for drain current measurements
- **Galvanic (optical) isolation of gate drivers (expensive)**

System Layout and Loop Inductance







- Module C has higher inductance added to the power loop and gate loop
- It results in slightly higher current unbalance but **less than 5%**
- Therefore, the system layout and loop inductance has **low impact** on Power Module paralleling

Load Impedance Impact

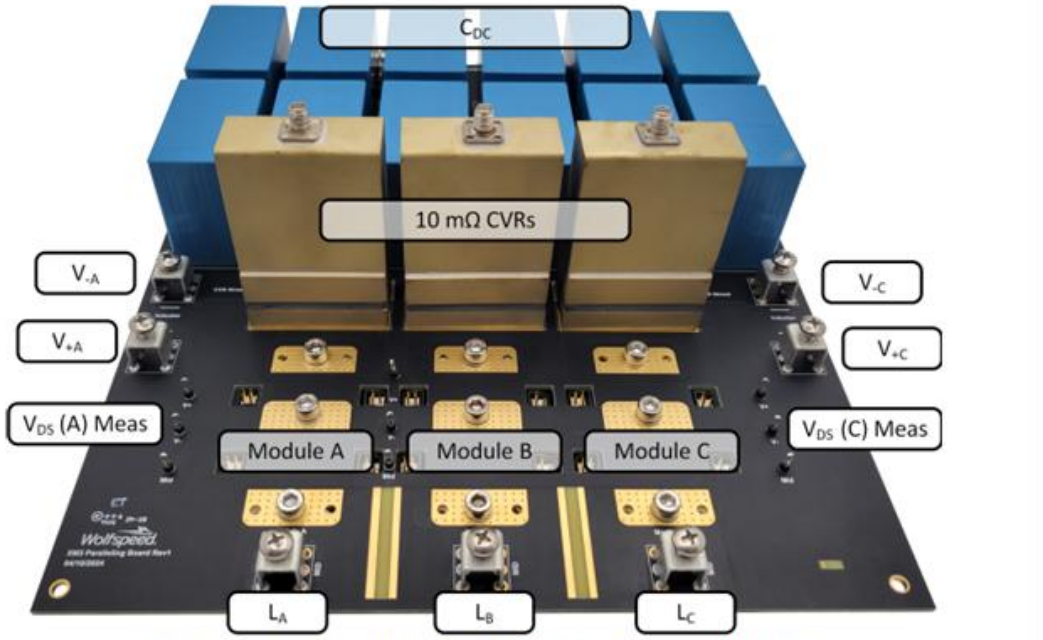
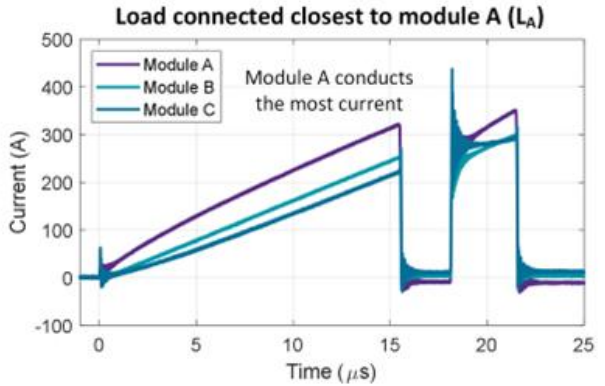
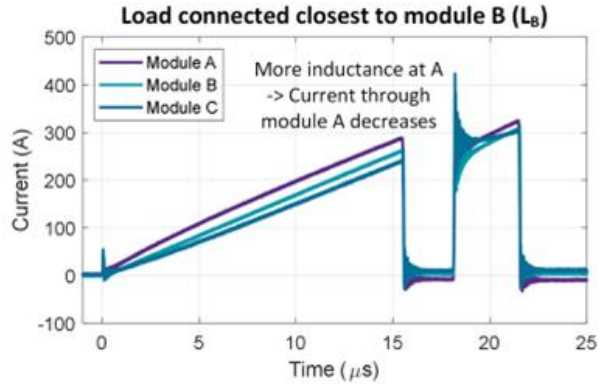
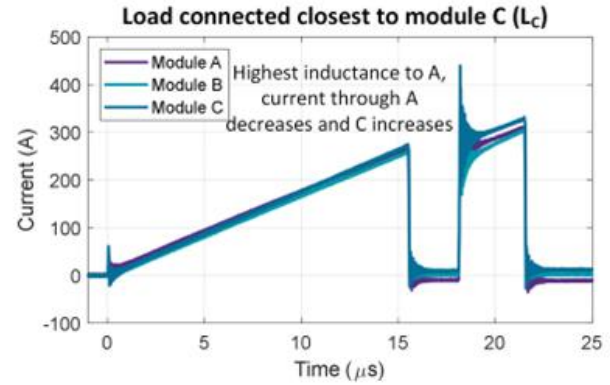


Figure 7: Paralleling study PCB (without gate drivers attached)

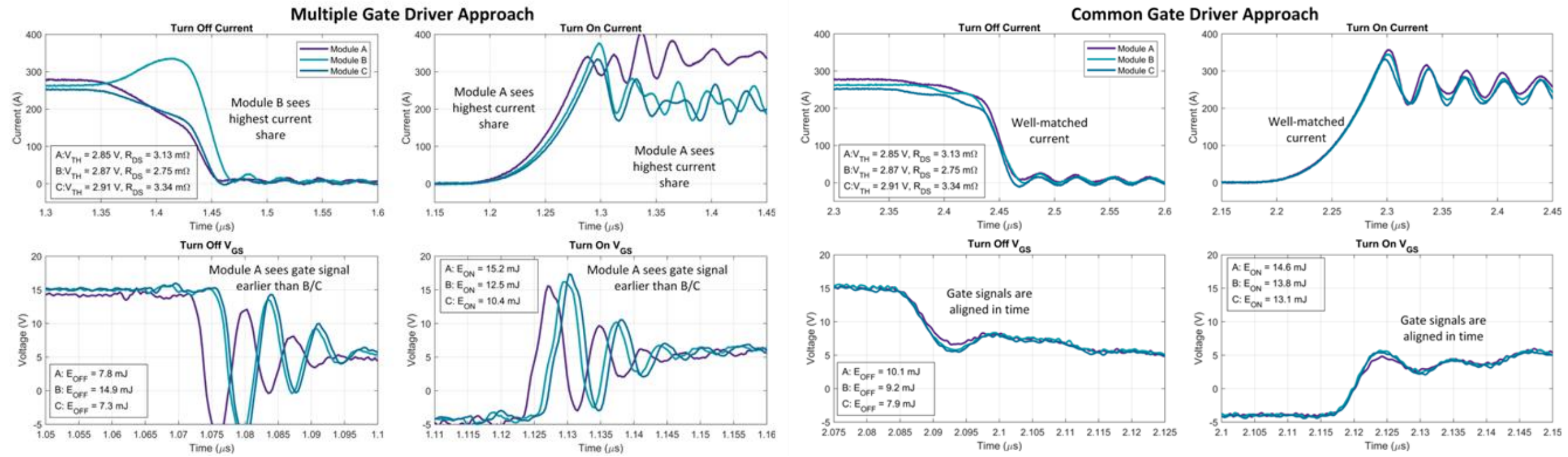






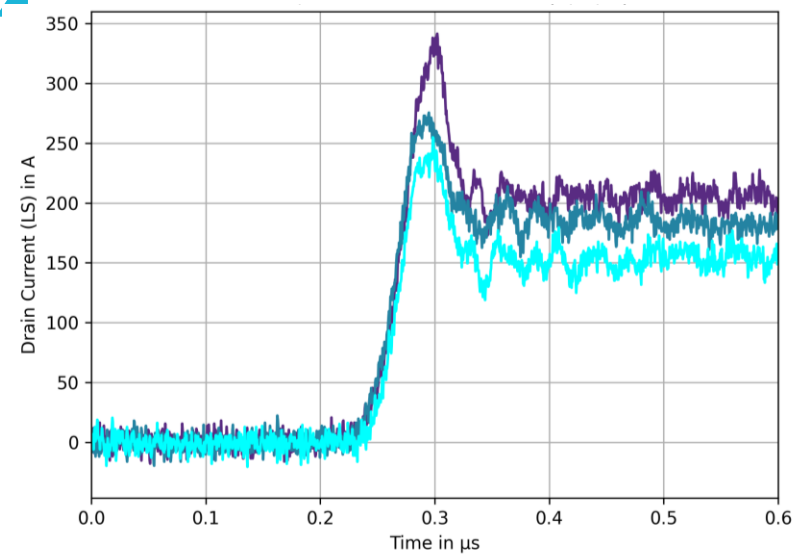
- The position of the load inductor is changed (L_A, L_B, and L_C) to add more inductance in path to the load from each module
- When the inductor is connected to L_A, the current through module A is significantly higher than through B or C
- As the load inductor is moved from L_A to L_B to L_C, the current through module A decreases and the current through module C increases

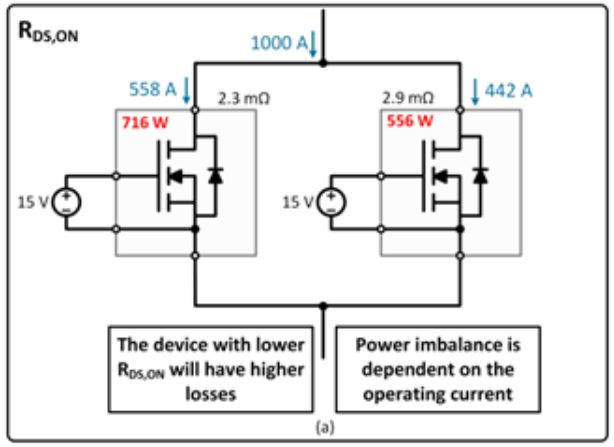
Gate Driver Configuration

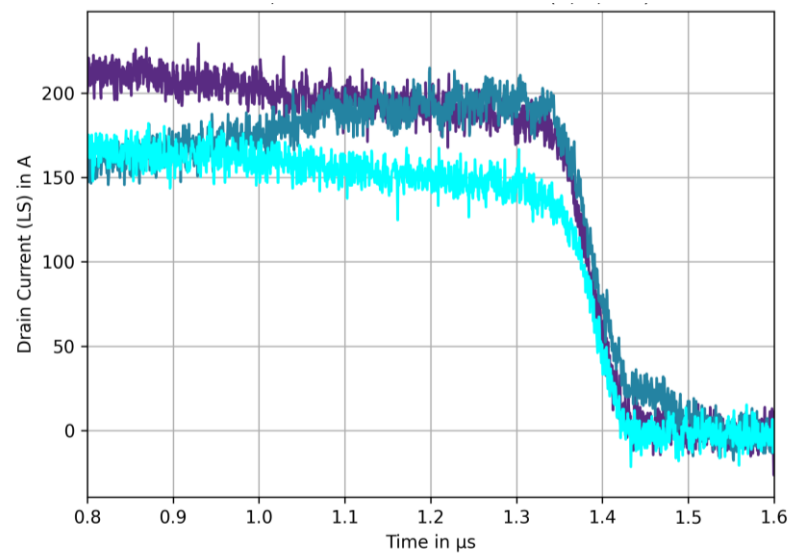


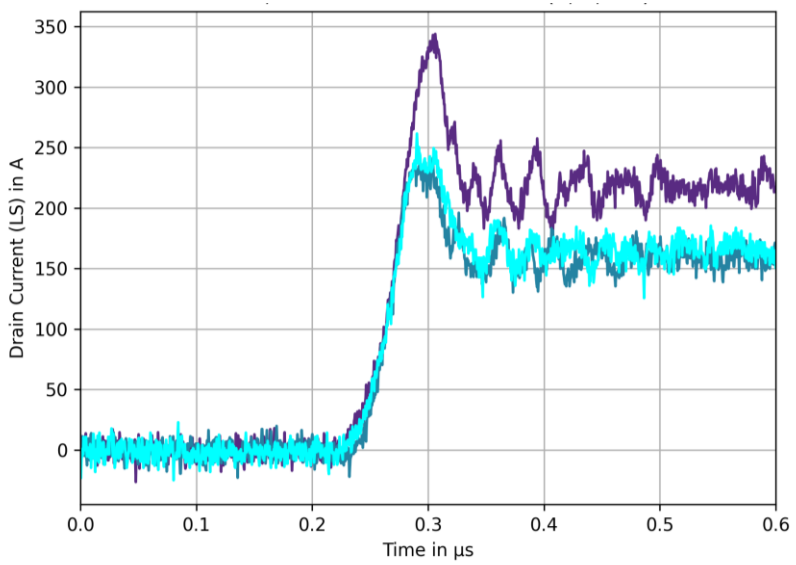
- The dynamic current matching and waveform quality is improved **significantly** with the common gate driver approach
- Inherent variation in signal timing and characteristics of components can cause significant imbalance between paralleled modules

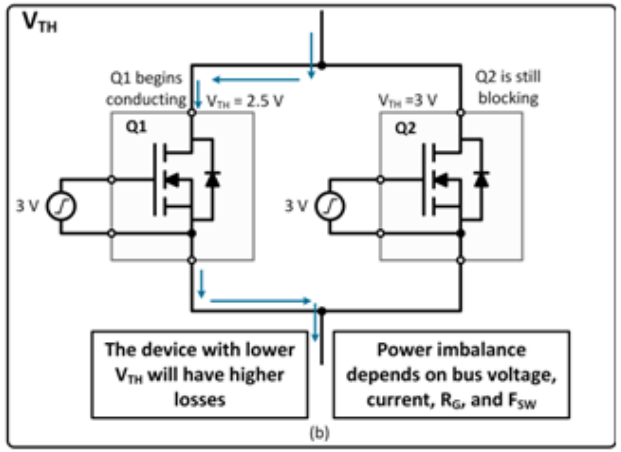
Module Parameter Mismatch

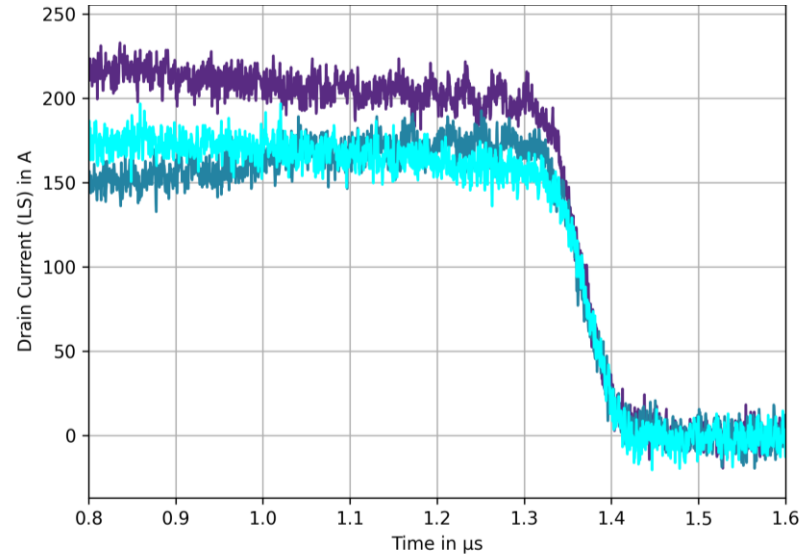












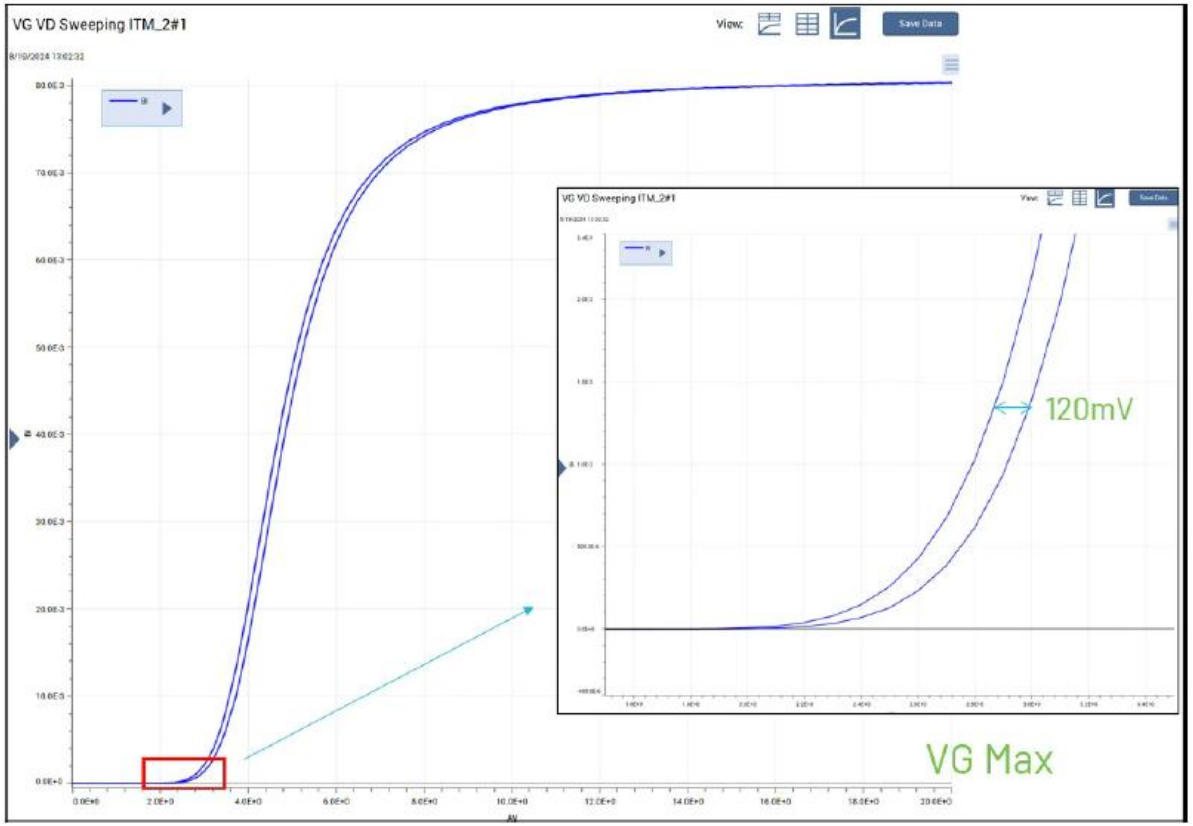
Summary of Factors Affecting Paralleling

Design Parameter	Importance for Dynamic Current Sharing	Comments
Power Loop Inductance Imbalance	Low	Power loop inductance should be minimized to reduce V_{DS} overshoot, but has minimal affect current sharing
Gate Loop Inductance Imbalance	Low	Gate loop inductance should be minimized to reduce V_{GS} overshoot, but has minimal affect current sharing
Load Impedance Mismatch	High	Modules should have a symmetric attachment to the load. Inserting inductance between each module and the load can reduce mismatch. Connect midpoints at the load, instead of at the bus
Gate Driver Implementation	High	Common gate driver implementations offer significantly better current sharing than distributed gate driver approaches. Propagation delay of signals
Module Characteristics	Medium	Increased V_{TH} imbalance between modules can increase dynamic mismatch. Before addressing this issue, ensure that the layout and gate driver implementations are optimized.

More details: Considerations for Current Balancing in Paralleled SiC Power Modules

Derive Precise Behavioral Models

I-V AND C-V CHARACTERIZATION



Tektronix

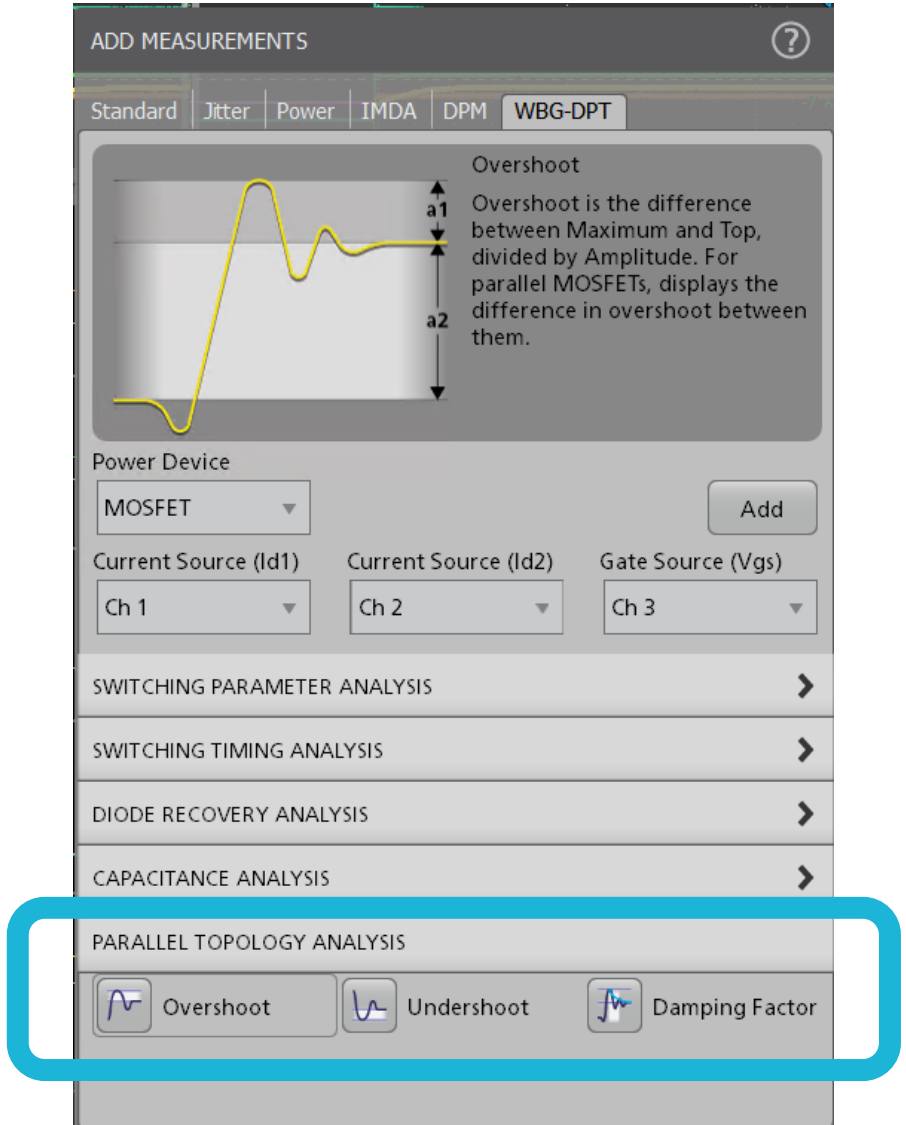
SiC MOSFET Threshold Voltage Testing Based on JEDEC JEP183A Using the 4200A-SCS Parameter Analyzer

APPLICATION NOTE

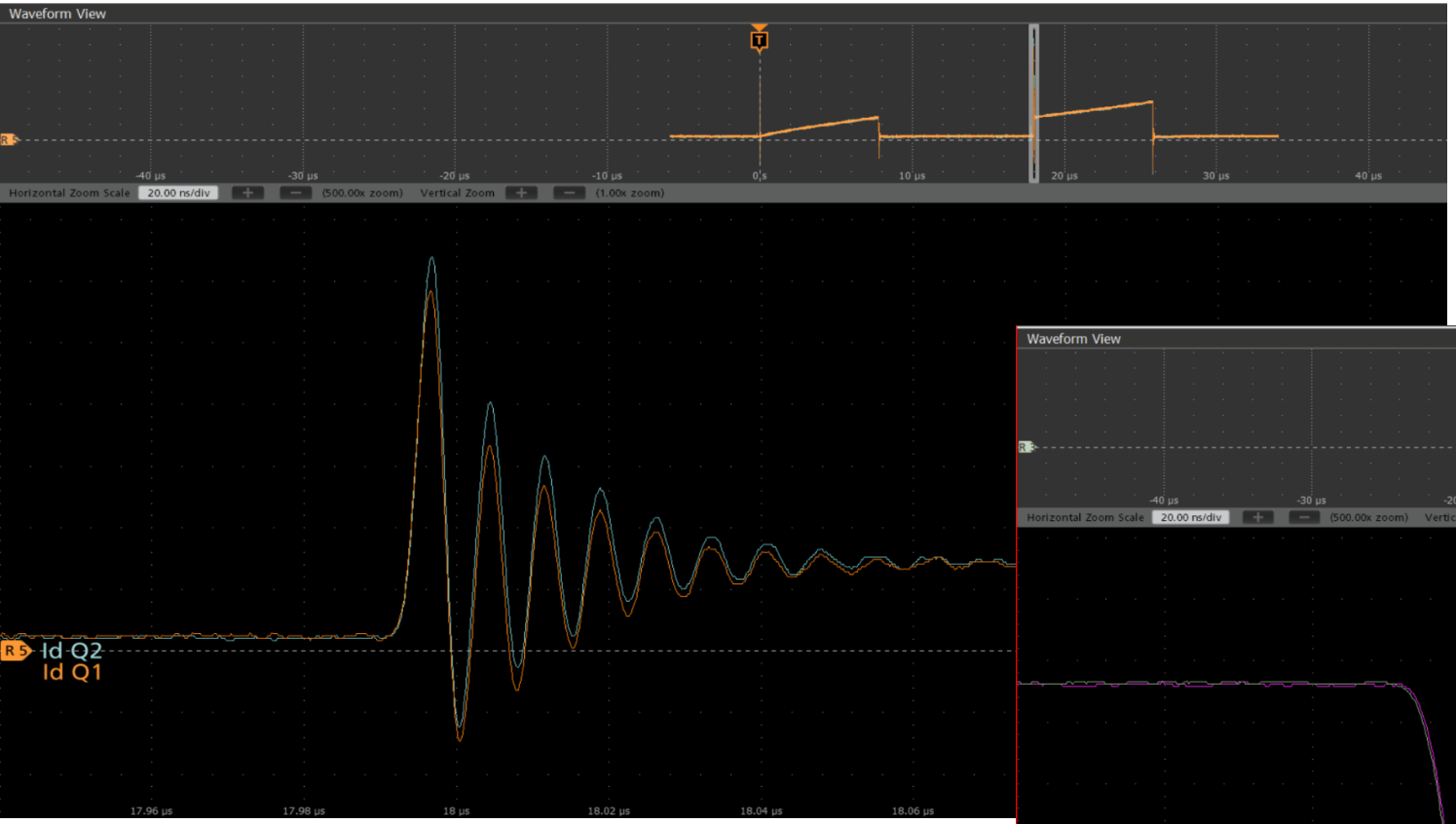
Experimental PCB Validation

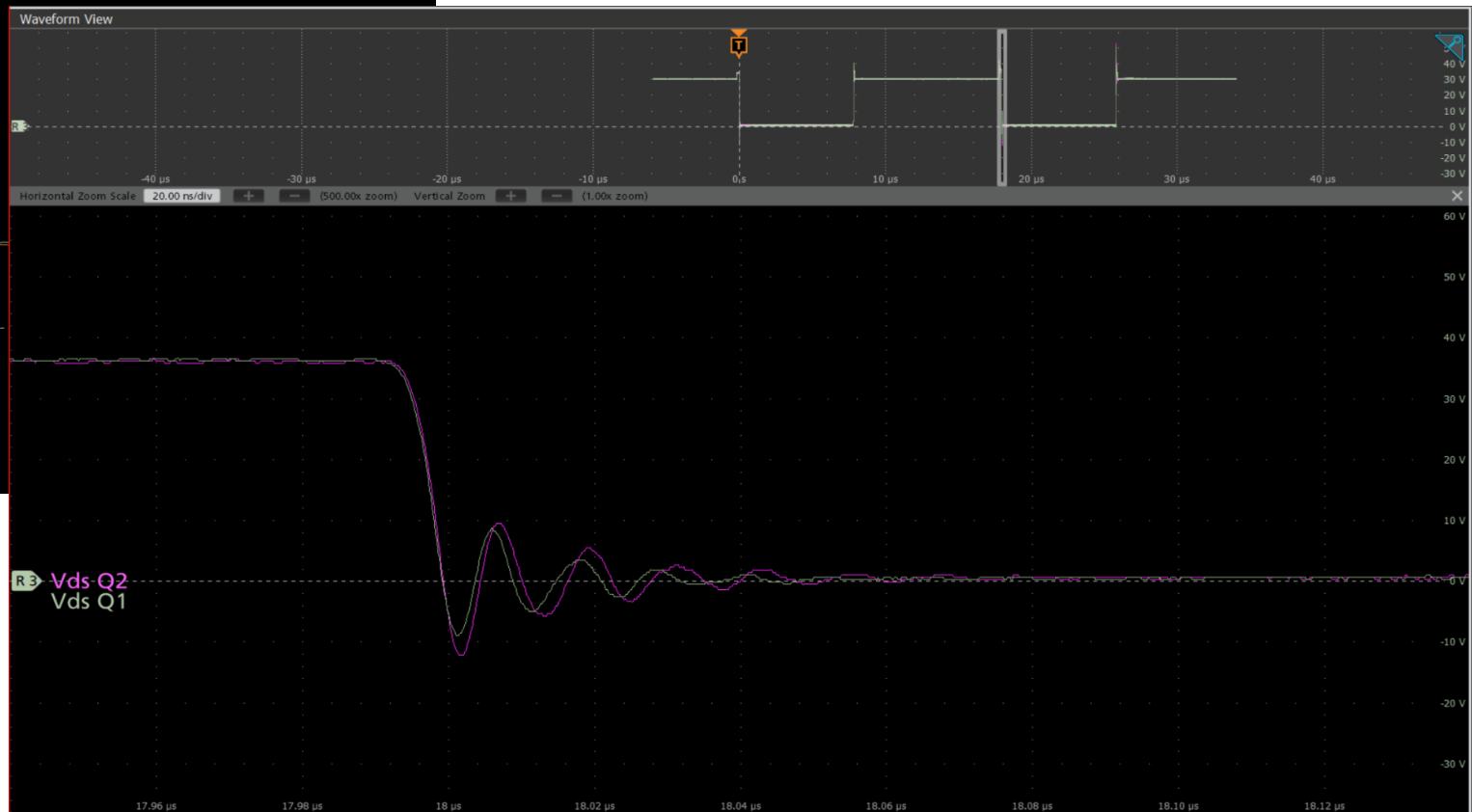
A NEW DEDICATED SOFTWARE CAPABILITY

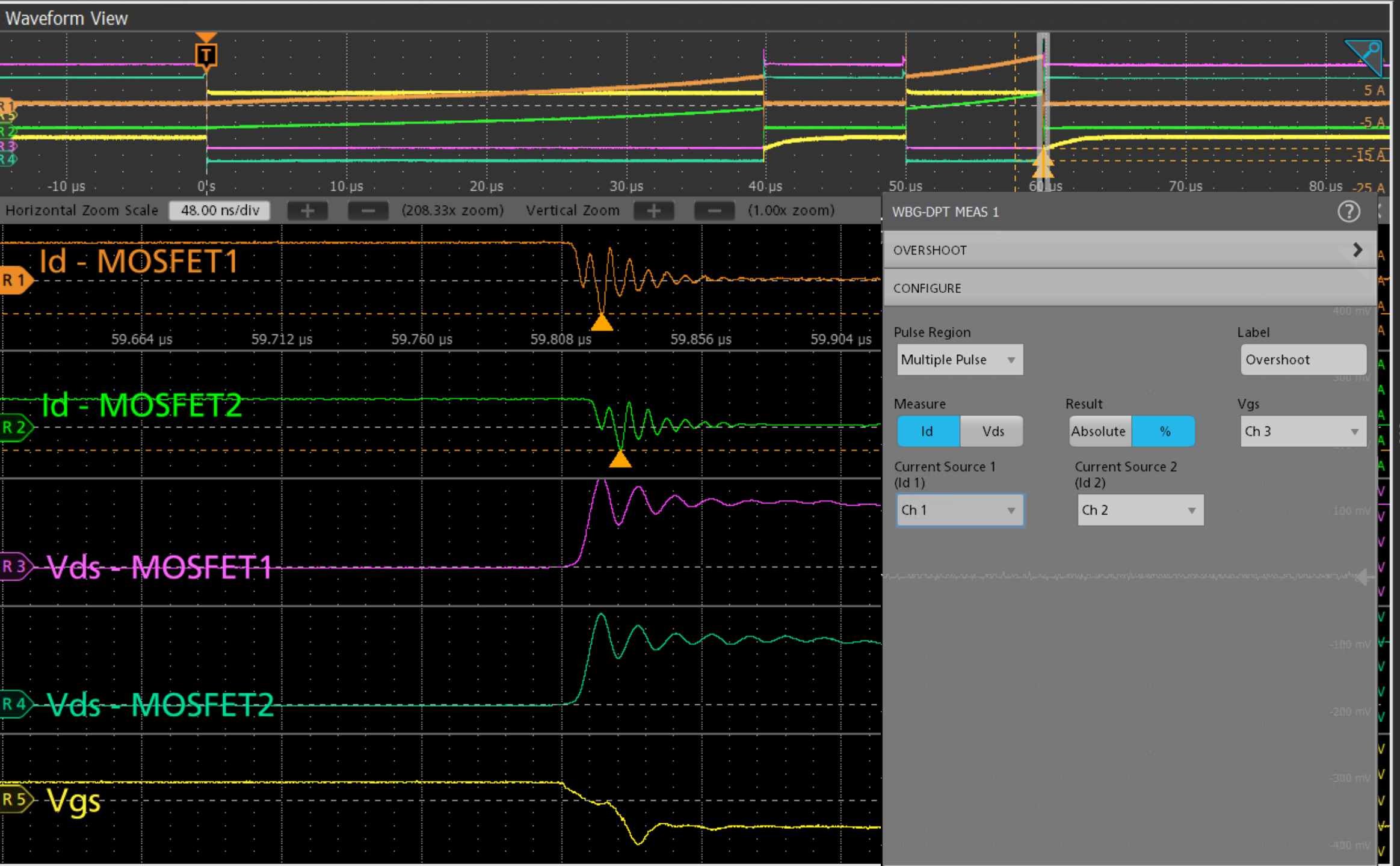
- Turn on / off waveforms under various load currents to detect current spikes and Vds variation rates
- Need multi-channel, high accuracy instrumentation and power probes
- Automated De-Skew
- Eon/Eoff
- Dead Time
- Overshoot/Undershoot Damping Factor

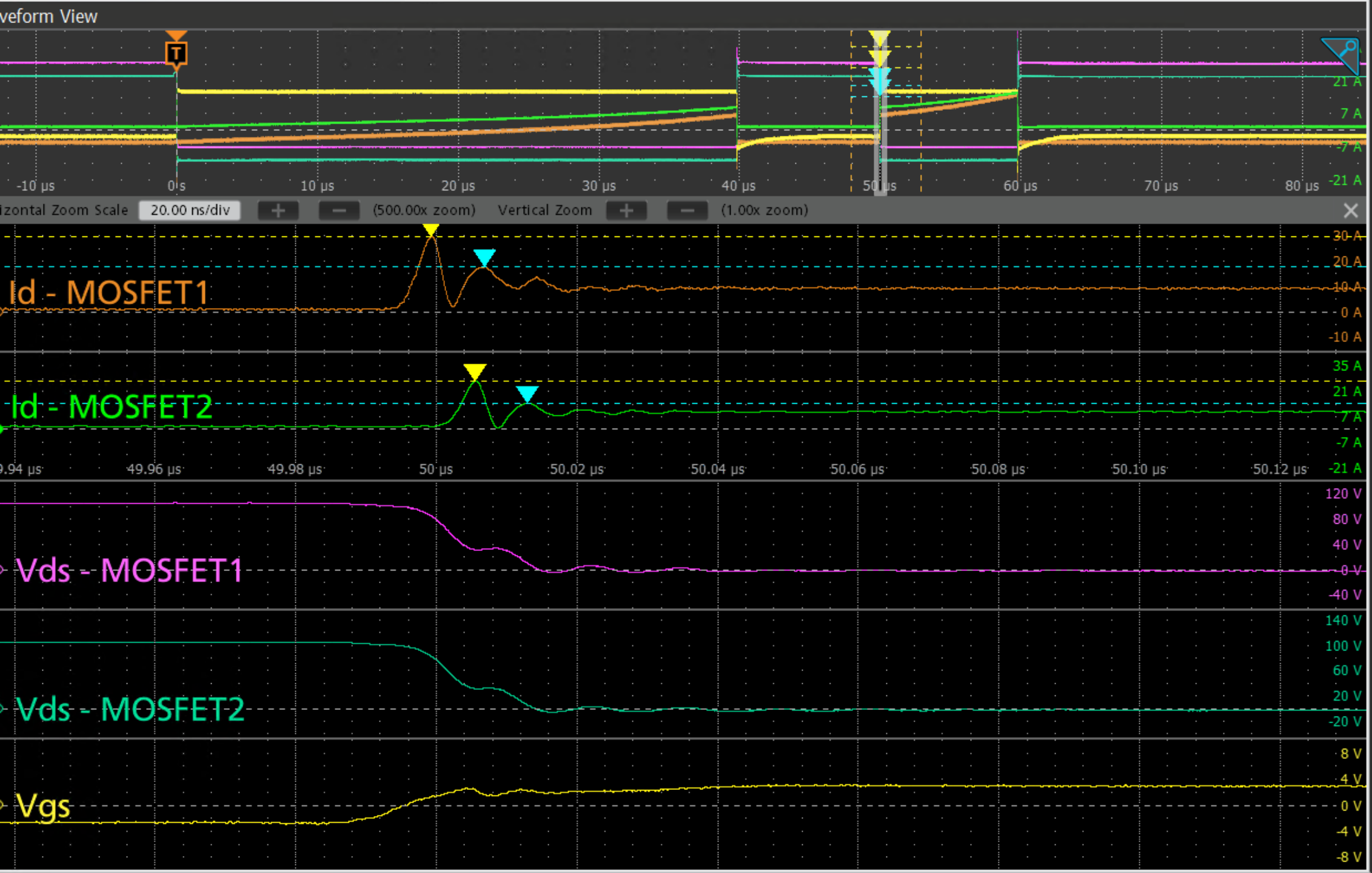


Overlapped Plots






Waveform View
5 A
-5 A
-15 A
-25 A
-10 µs
0 s
10 µs
20 µs
30 µs
40 µs
50 µs
60 µs
70 µs
80 µs
Horizontal Zoom Scale
48.00 ns/div
(208.33x zoom)
Vertical Zoom
(1.00x zoom)
Id - MOSFET1
R 1
59.664 µs
59.712 µs
59.760 µs
59.808 µs
59.856 µs
59.904 µs
Id - MOSFET2
R 2
Vds - MOSFET1
R 3
Vds - MOSFET2
R 4
Vgs
R 5
WBG-DPT MEAS 1
OVERSHOOT
CONFIGURE
Pulse Region
Multiple Pulse
Label
Overshoot
Measure
Id
Vds
Result
Absolute
%
Vgs
Ch 3
Current Source 1
(Id 1)
Ch 1
Current Source 2
(Id 2)
Ch 2
400 mV
300 mV
100 mV
-100 mV
-200 mV
-300 mV
-400 mV
Add New...
Cursors
Measure
Results Table
Meas 1
R1
Undershoot'
Id 1: 100.5 %
Id 2: 102.3 %
Δ12: 1.848 %



Add New...

Cursors | Callout

Measure | Search

Results Table | Plot

More...

Meas 3 R1

Damping Factor'

Id 1:	128.4 m
Id 2:	188.3 m
$\Delta\zeta_{12}$:	59.82 m
Δt_1:	7.600 ns
Δt_2:	7.440 ns

Values':

Id 1:	128.437 m
Id 2:	188.255 m
$\Delta\zeta_{12}$:	59.818 m
Δt_1:	7.600 ns
Δt_2:	7.440 ns

THANK YOU

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Technical Marketing

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