Silicon Carbide JFETs enable breakthroughs of high-voltage solid state power distribution

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Bodo‘s Wide Bandgap Event 2025

Making WBG Designs Happen

SiC

Solid State Power Distribution

Why to change a 100-year old, proven electro-mechanical concept

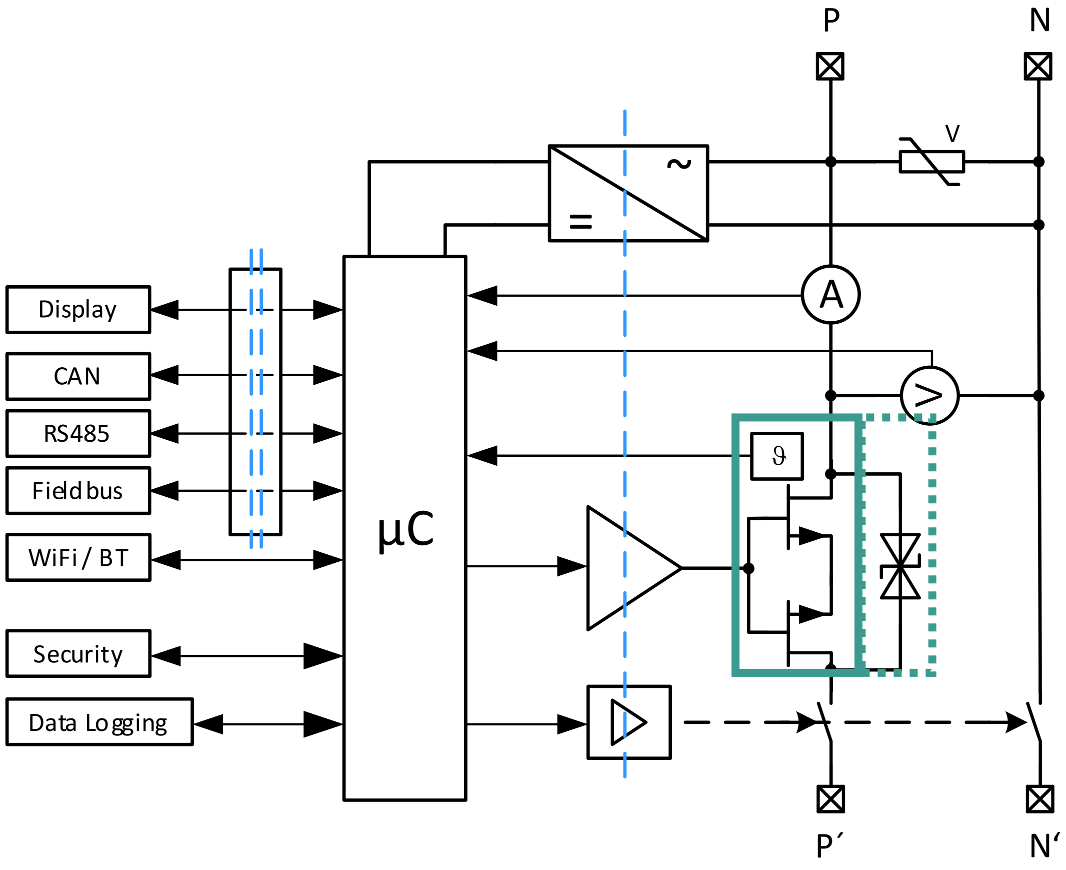
- **Reduction of Fault isolation delay from >10 ms to <5 µs**
  - Minimal current overshoot
  - Reduced Distortion in the distribution grid
  - Selectivity vs. Electronic Sources
- **Smart Protection Mechanisms**
  - Auto-Retry / Failure Recovery
  - Smart Inrush Handling
  - Self Diagnostic
- **Arc-Free, Wear-free Actuation and Protection**
  - Reduced Maintenance
  - Installation Space (IT environment)
  - Smart Load Control
- **AC and DC compatible**

- **Size / Ampacity**
- **Power Dissipation**
- **Cost (CAPEX)**

→ **Enabled by Power Semiconductor Solutions**

Solid State Circuit Breakers from a System Perspective

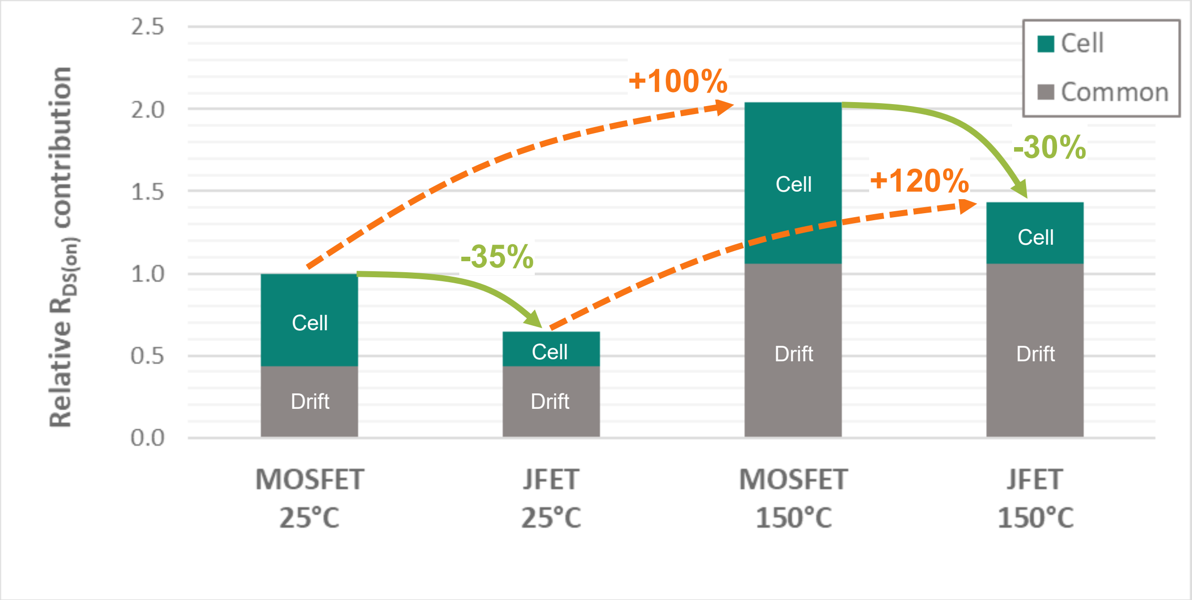
Power Stage as critical building block



SSCB Requirement	Example: 63A/800 Vdc
– Very low Voltage drop @ rated current	– 150 mV/Pole 2.3 mΩ total
– Overload Capability	– 3x I_{nom} * 2s
– High Current Switching Capability	– I_{SD} = 1 kA
– Interplay with Clamping Device	– TVS
– Overvoltage / Overcurrent Robustness	– OVC III
– Power Temperature Cycle Robustness	– 500kc @ 125 °C
– Miniature Solution Size	– Equivalent to 63A MCB
– Lifetime equivalent to EM solution	– >20 years * 24/7

JFET: Advancements in Ron*A and FBSOA

R_{DSon} Contribution: 1.2kV CoolSiC™ MOSFET vs. JFET

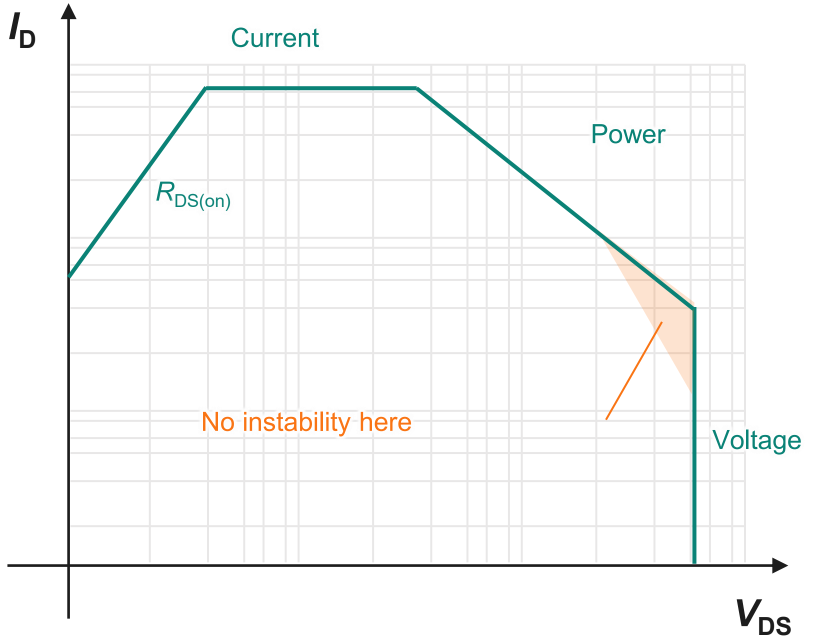


Best-in-Class RDSon Ratings:

2.3mΩ @ 1200V V_{BDss}

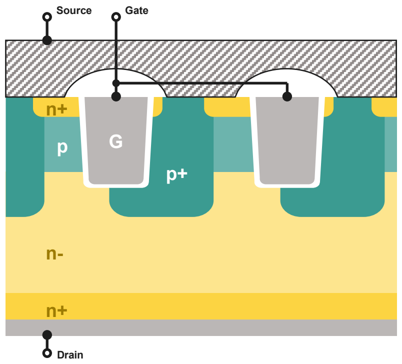
1.5mΩ @ 750V V_{BDss}

JFET FBSOA: ID vs. VDS

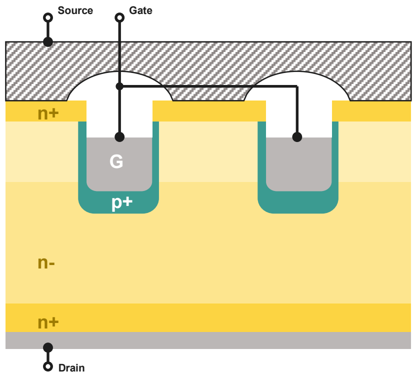


- Thermal Stability under all operating conditions
  - No hot-spotting during overload pulses
  - Linear mode capable
  - Stable operation in “avalanche”

Technology differentiation – CoolSiC™ JFET vs. MOSFETs



SiC MOSFETs

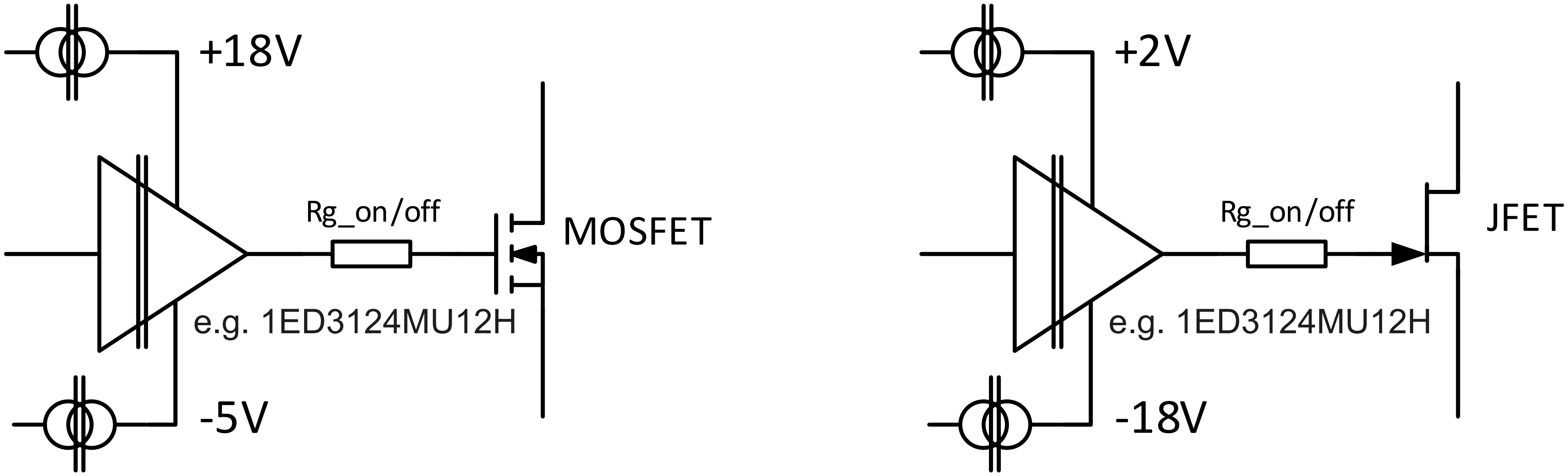


SiC JFETs

Construction	Channel conduction, normally off Fully isolated gate Optimized for minimum gate feedback	Bulk conduction, normally on Non isolated gate Optimized for $R_{DS(on)}$ and robustness
FOMs	Relatively high(er) $R_{DS(on)}$ Lower temperature coefficient	Lowest possible $R_{DS(on)}$ per device Higher temperature coefficient
Benefits	Simplified control, high switching speed Compatibility to legacy circuits	Maximum power density Active clamping Linear mode operation

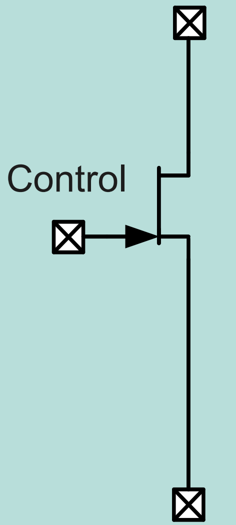
Driving a CoolSiC™ JFET is easy…

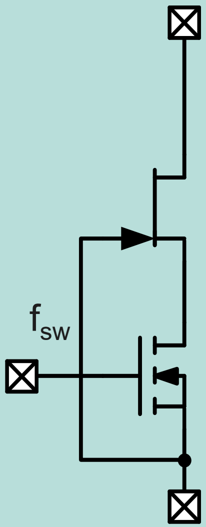
Example: Isolated Gate Drive Scheme

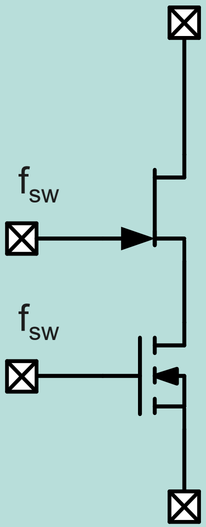


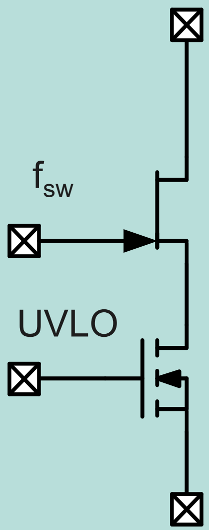
- Exchange Polarity of Supply voltages: +18V → -18V; -5V → +2V
- Adoption of Rg_on and Rg_off values
- Use of same (basic) Gate Driver

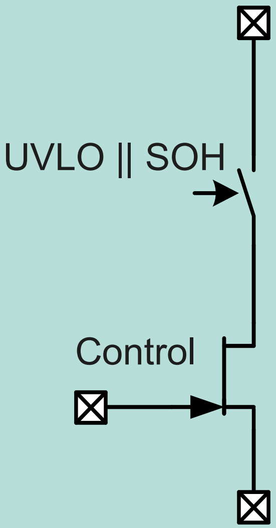
Drive modes and application mapping for JFET/JFET Cascodes

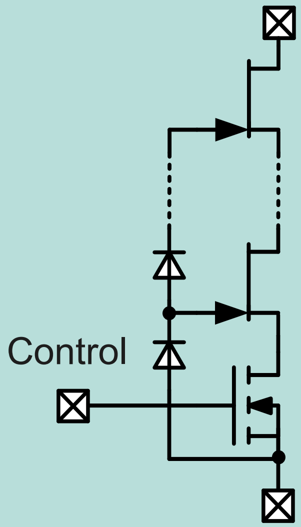












Topology	Bare Bone	Cascode	Direct Drive	Safety Cascode	SSCB w/ airgap and safety disconnect	Super Cascode
Application	› Motor starters › Drives	› SMPS	› SMPS › Drives	› eFuse › SSCBs › Drives	› SSCBs	› HV-SSCBs

Package Optimization for full application performance

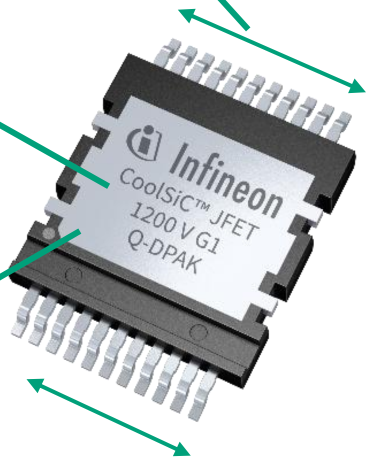
Q-DPAK enables efficient system integration into SSCB assemblies

Large Drain and Source interface area

- Minimize Losses
- Reduced current density at the interface

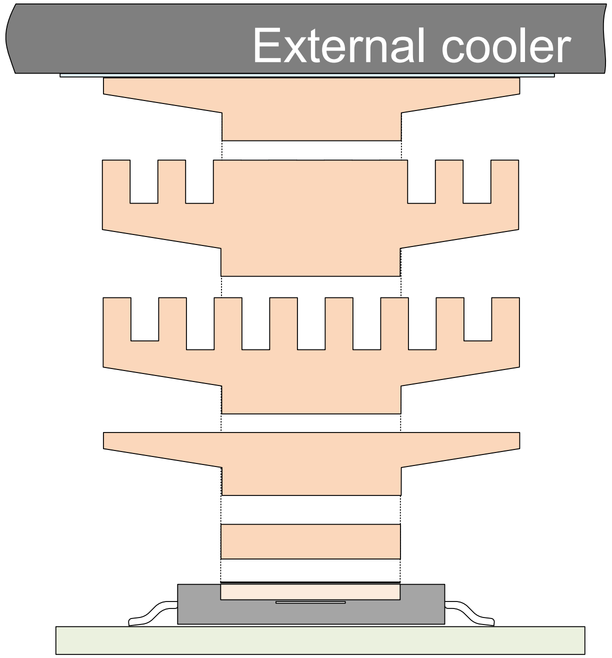
Optimized internal construction

- High current interfaces
- Diffusion soldering
- Large die area & internal paralleling



Top-Side Cooling & large heatslug

- Lowest possible R_{th}
- Directly connected, local C_{th}
- Application-adjustable C_{th}



- Directly attached TSC cooler enables flexibility
  - Adjust i²t capability via C_{th} extension
  - Optimize R_{th}
  - Reduce Thermal cycling stress

Summary

- Solid-State Power Distribution is a new emerging application field with special requirements to the applied semiconductors
  - Ultra-Low RDSon of HV Power Transistors
  - Robustness and Reliability under heavily exposed conditions
- The CoolSiC™ JFET enables high performance SSCB designs by
  - Groundbreaking low R_{DSon} values
  - Simplified device paralleling
  - High Current Avalanche Ratings to minimize the effort in clamping solutions
- The Q-DPAK Package is optimally suited for the implementation of high current SSCBs
  - Large routing interface area on both, Drain and Source contacts
  - Large thermal interface area
  - User-extendable thermal capacitance for overload capability.

Infineon