Selecting the Right SiC MOSFET Device for Soft-Switching Converters: What Really Matters

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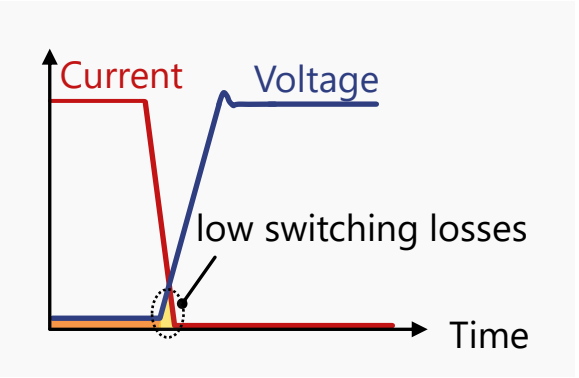
Making WBG Designs Happen

SiC

Motivation

- Zero-voltage switching (ZVS) in power converters can enhance system efficiency while also being able to mitigate electromagnetic interference
- ZVS is achieved by minimizing the voltage-current overlap using circuit parasitics or passive-reactive components
- Switching losses are significantly reduced by over 90% compared to hard-switching, but residual losses remain during turn-OFF transitions
- Residual switching losses depend on transistor parameters and gate-driver properties



→ **Goal: Identify the optimal power semiconductor for ZVS applications operating at up to several hundred kilohertz**

Test Methodology

- Transistors operated for five seconds using Triangular-Current-Mode (TCM) modulation
- Total power losses measured by a **transient calorimetric method**
- **Temperature changes ($\Delta\vartheta/\Delta t$)** precisely captured using high-precision **thermal imaging**
- Total losses calculated: $\boxed{P_{\text{loss,total}} = C_{\text{th}} \frac{\Delta\vartheta}{\Delta t}}$
- Thermal capacitance C_{th} determined through dc-calibration
- Copper block soldered onto the transistor's backside to increase thermal capacitance and measurement accuracy
- Parallel-connected SiC Schottky diodes prevent distortion of measurement results

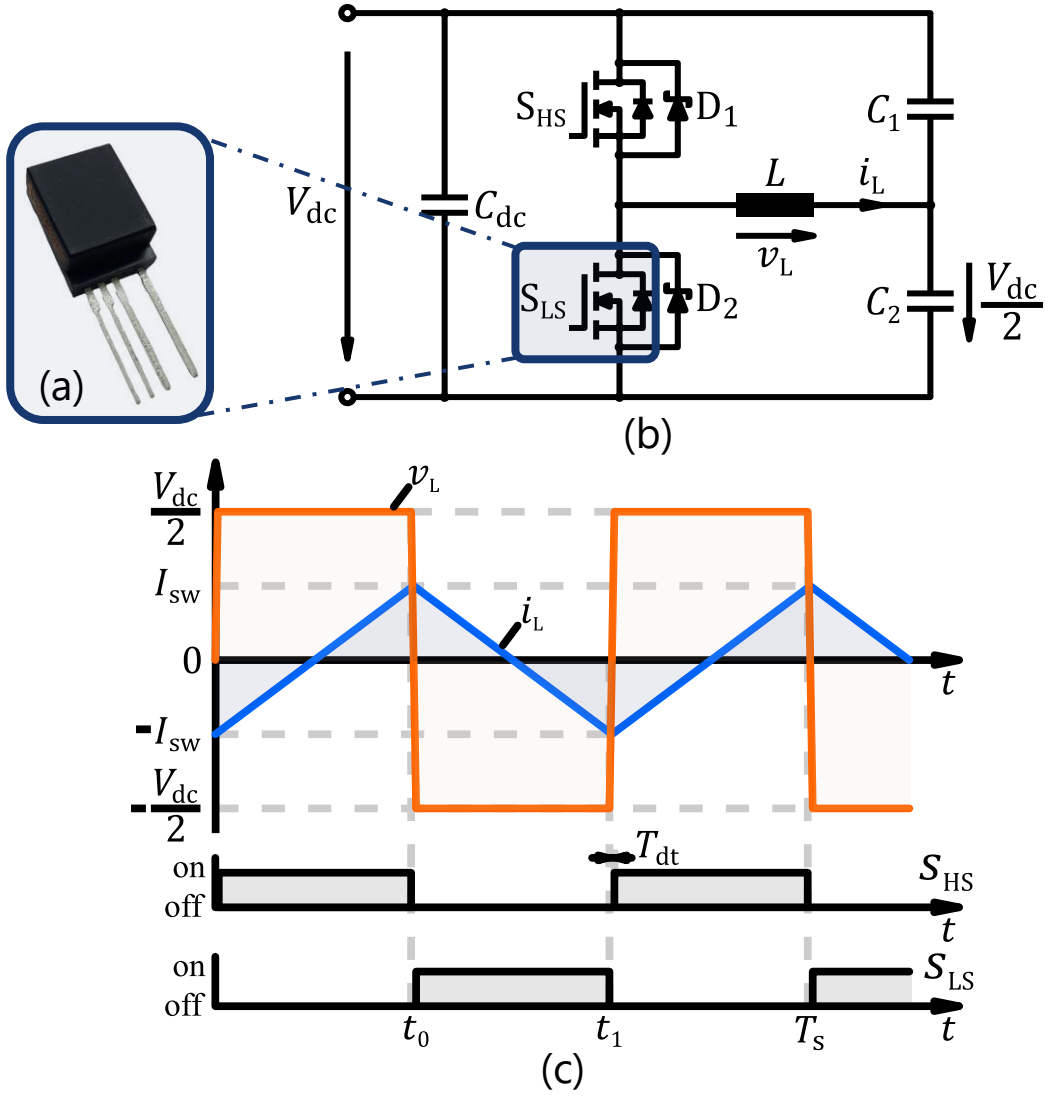


Fig. 1: (a) Black-painted copper block (15 grams) soldered to a transistor. (b) Circuit diagram of the experimental setup featuring two transistors under evaluation. (c) Applied TCM modulation.

Experimental Circuit and Test Parameters

Parameter / Component	Value
DC-link voltage V_{dc}	800 V
DC-link capacitance C_{dc}	40 µF
DC-link capacitance $C_1 = C_2$	20 µF
Inductance L	[14 28 61] µH
Gate turn-on voltage $V_{gs(ON)}$	18 V
Gate turn-off voltage $V_{gs(OFF)}$	– 5 V
Gate resistor $R_{g(ON)}$ / $R_{g(OFF)}$	4 Ω / 0 Ω
Dead-time T_{dt}	120 ns
SiC Schottky diode D_1, D_2	Sanan SDS120J002D3

- The transistors' dead-time is kept as short as possible to minimize the current flowing through the intrinsic body diodes
- A SiC SBD is connected in parallel with each transistor to further minimize conduction losses in the body diode during the dead-time
- Three different inductance values used to evaluate power losses at various switching frequencies

Specifications of the SiC Transistors with TO-247-4 Package under Evaluation

- **T1**: Planar-structured **Sanan SiC MOSFET SMS1200016M**
- T2 … T10: Other commercially available semiconductor devices of the latest generations
- All devices tested have a blocking voltage of 1200 V and a similar $R_{ds,(ON)}$

ID	Device	Structure	$R_{ds(ON)}$ in mΩ	$R_{g,int}$ in Ω	C_{iss} in nF @ V_{ds} = 1 V	C_{oss} in nF @ V_{ds} = 1 V	V_{th} in V	$\tau_{g(OFF)}$ in ns ($R_{g,int} \cdot C_{iss}$)
T1	SiC MOSFET	Planar	16	0.9	7.2	5.8	2.8	6.5
T2	SiC MOSFET	Planar	15	1.1	6.3	8.9	4.0	6.9
T3	SiC MOSFET	Planar	11	1.2	7.7	5.8	2.7	9.2
T4	SiC MOSFET	Unknown	21	0.8	6.7	5.3	2.5	5.4
T5	SiC MOSFET	Planar	14	1.4	9.1	6.4	3.0	12.7
T6	SiC MOSFET	Trench	14	3.7	5.4	3.9	4.2	20.0
T7	SiC MOSFET	Planar	14	2.6	8.5	4.6	2.5	22.1
T8	SiC MOSFET	Trench	17	3.0	3.3	3.1	4.2	9.9
T9	SiC MOSFET	Planar	15	1.6	5.9	5.7	3.1	9.4
T10	SiC JFET Cascode	Planar	16	0.8	9.1	25.2	4.7	7.3

Device parameters were obtained from datasheets or measured under consistent and comparable test conditions.

Experimental Results

- Temperature data recorded by thermal imaging camera with an average sample rate of 15 Hz)

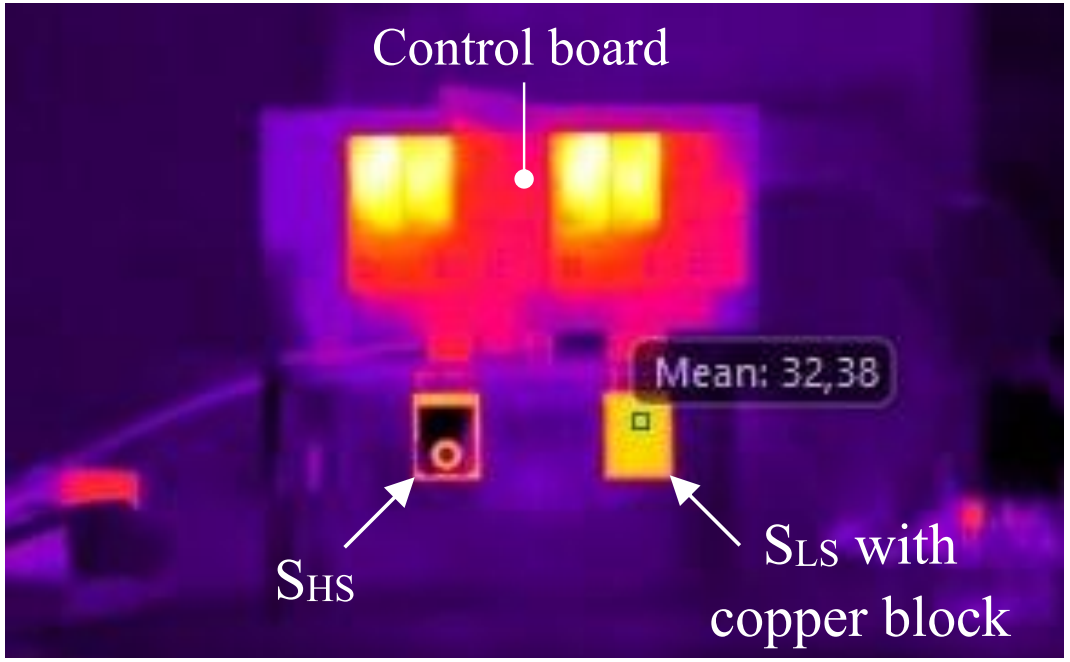


Fig. 2: Thermal imaging of a heating process.

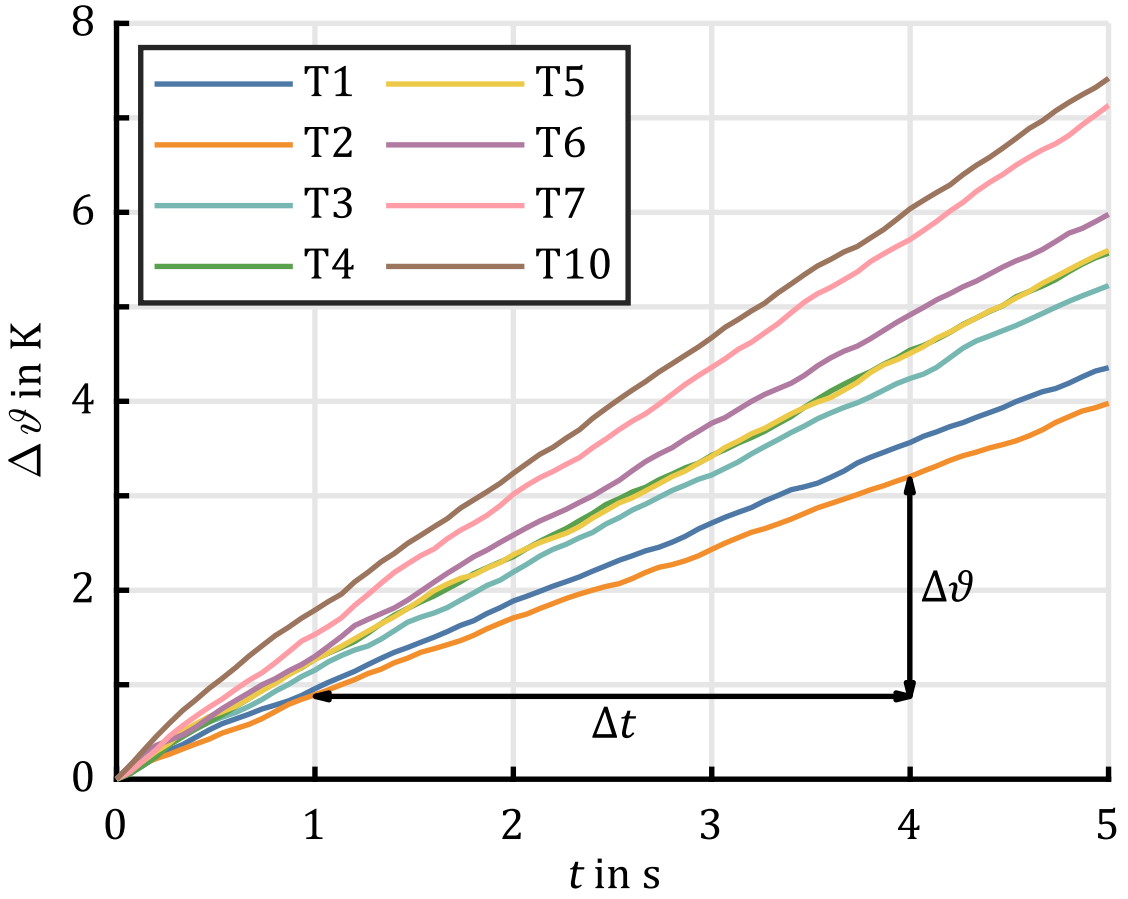


Fig. 3: Measured copper block temperature profiles over five seconds for various transistors switching at 40 A.

- Total power losses are determined by the slope of the thermal profiles and the thermal capacitance

Experimental Results

- Switching losses are derived from total losses minus conduction and gate losses
- T1 and T2 superior due to rapid gate discharge (short time constant $\tau_{g(OFF)}$)
- T2 performed best: higher output capacitance C_{oss} slows V_{ds} rise, further reducing losses
- SiC JFET Cascode device is less effective due to limited external control over turn-OFF speed
- Negative gate turn-OFF voltage had a minor influence
- External capacitance dominates C_{oss} in most practical ZVS converter applications

→ **Internal gate resistance and input capacitance are critical for minimizing residual switching losses!**

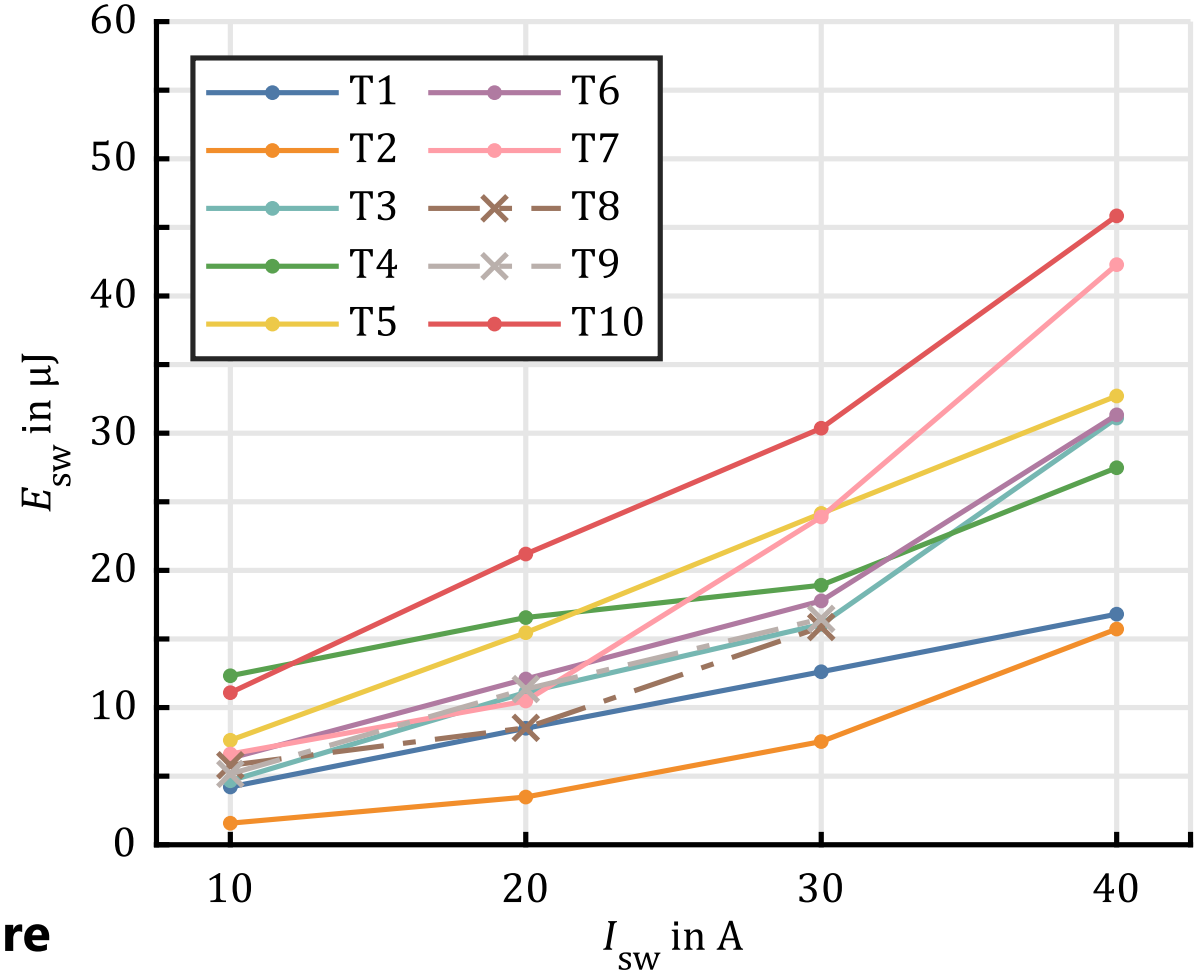


Fig. 4: Calculated residual switching energies for the evaluated devices at different switched currents.

THANKS

Further literature: T. Lehmeier, Y. Zhou, M. März, and A. P. Pai, “Influence of SiC MOSFET Device Parameters on Zero-Voltage Switching Losses,” in Proc. PCIM Europe, Nuremberg, Germany, 2025, pp. 1928–1934, 10.30420/566541254, https://ieeexplore.ieee.org/document/11053453.

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