Paralleling SiC MOSFETs: a robust approach for high-power converter performance and thermal management

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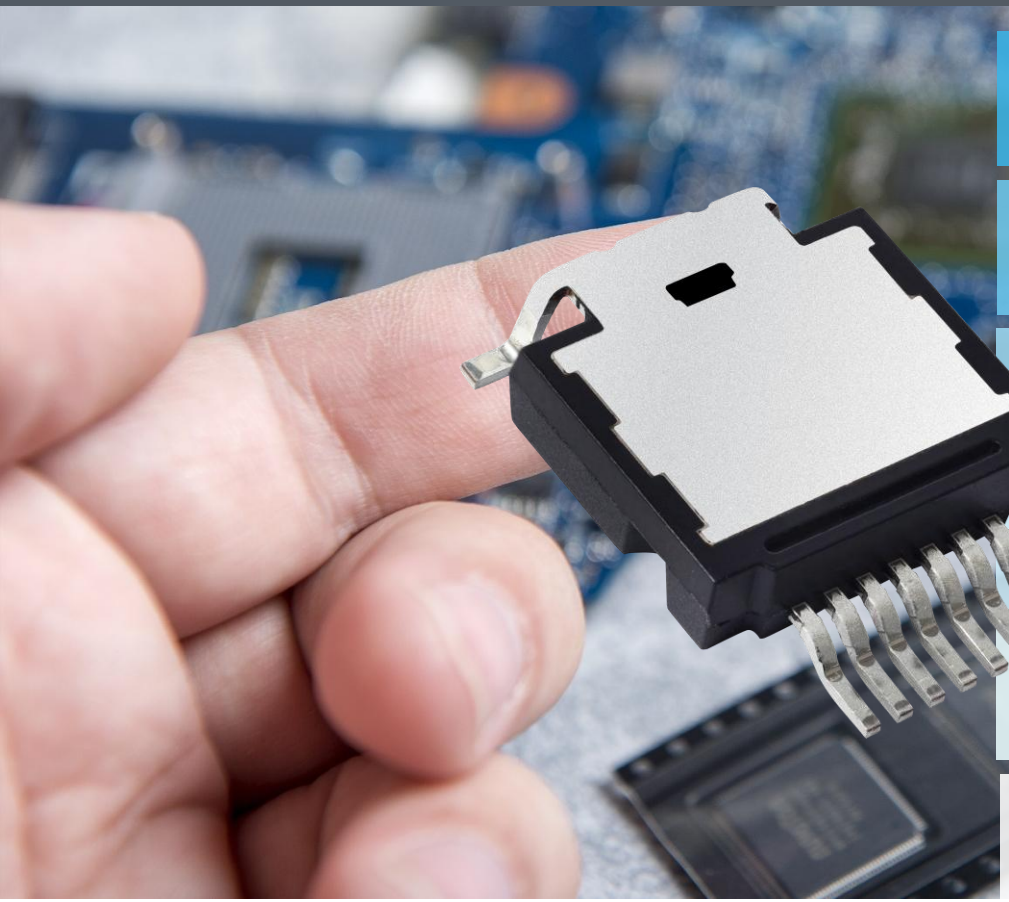
Bodo's Wide Bandgap Event 2025

Making WBG Designs Happen

SiC

SiC MOSFET - packaging

Research in advanced package technologies



Leadless packages
Enablers for miniaturization

Leaded packages
Std packages for economy of scale

Top-side cooling SMD
Connected on heatsink for excellent cooling

Multisintering package
High reliability, high power density

Modular package
Multipurpose configurations

Bare dice
High-temperature or in-house assemblies

PowerFLAT 8x8 HV TO-LL

Q3‘26

HiP247 HiP247-4 H2PAK-7 TO247-4 HC

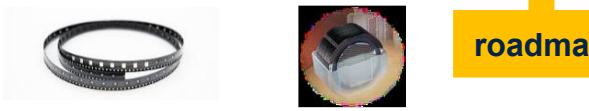
HU3PAK* HU3PAK HC

Q2‘26

STPAK*

ACEPACK* SMIT ACEPACK* 1, 2 & 3

roadmap



Tested dice in T&R Wafer on Sticky foil

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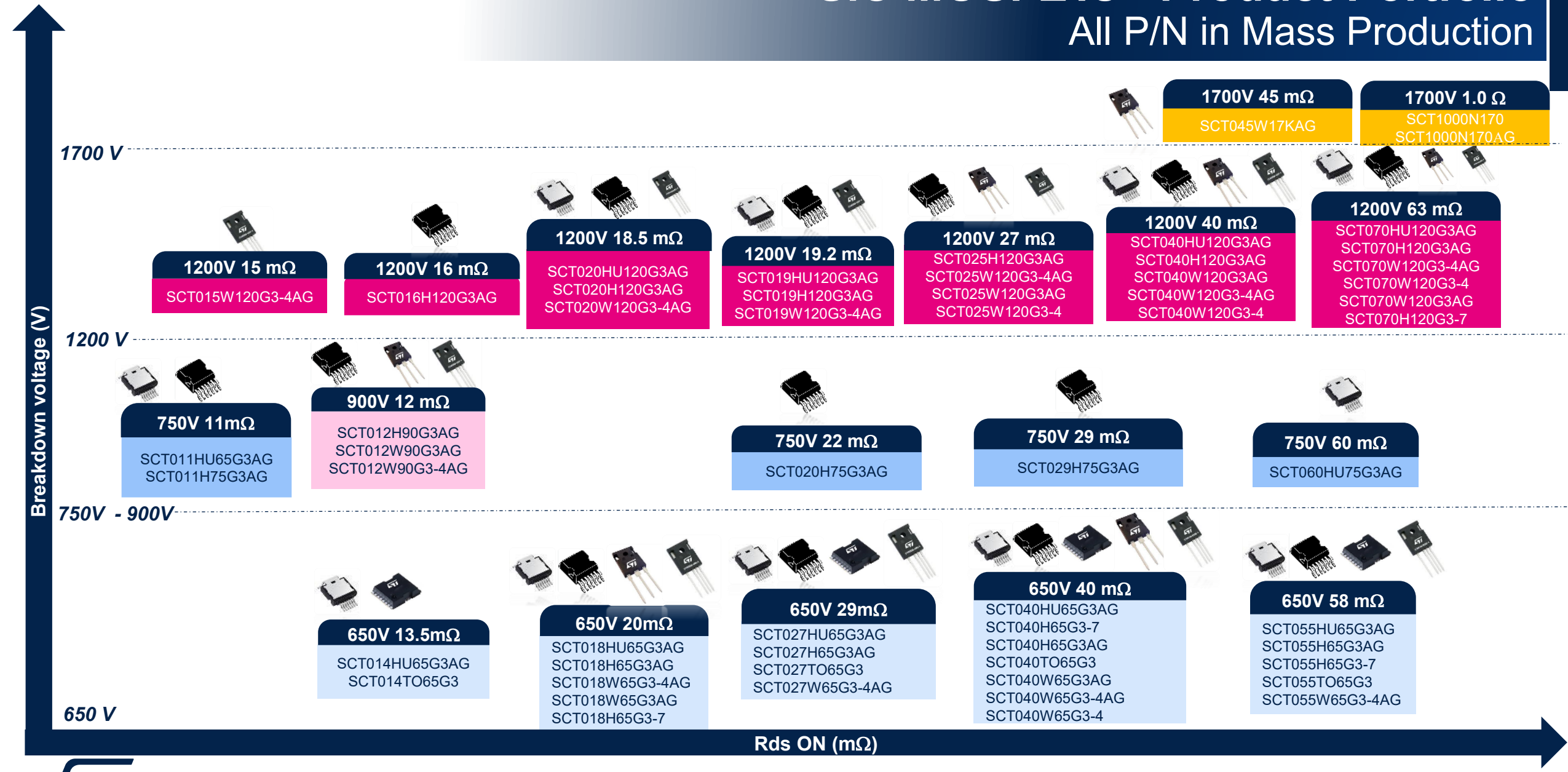
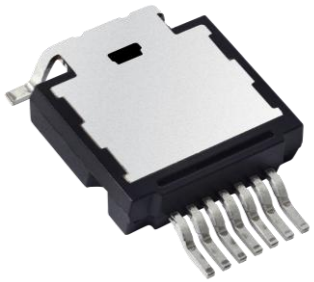
SiC MOSFETs - Product Portfolio
All P/N in Mass Production



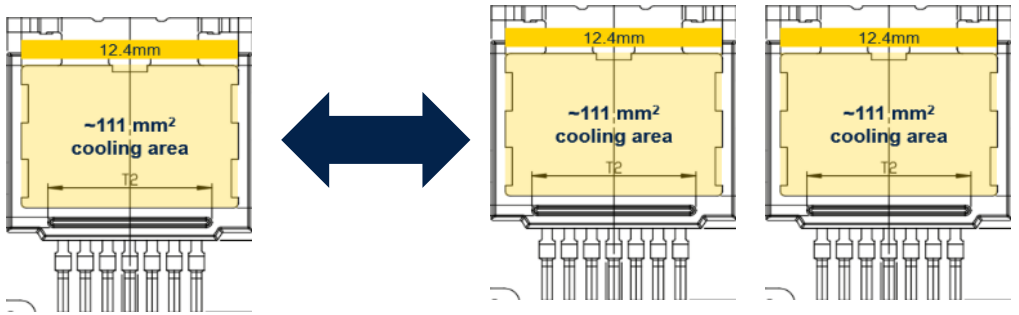
Power Switch Parallelization

Why we talk about parallelization?

Benefits of parallelization
1. Thermal



HU3PAK



Devices	Total Rdson (Configuration)	Equivalent Thermal resistance J-case	Equivalent Thermal resistance case-heatsink*	Equivalent Total thermal resistance Junction-heatsink	ΔTj for each 100 W Power Losses
SCT019HU120G3AG	**9.6 mΩ** (2 x 19.2mΩ in //)	0.15°C/W (2 x 0.3 in //)	0.3°C/W (2 x 0.6 in //)	0.45°C/W (2 device in //)	45°C
SCT025HU120G3AG	**13.5 mΩ** (2 x 27mΩ in //)	0.2°C/W (2 x 0.4 in //)	0.3°C/W (2 x 0.6 in //)	0.5°C/W (2 device in //)	50°C
SCT040HU120G3AG	**20 mΩ** (2 x 40mΩ in //)	0.25°C/W (2 x 0.5 in //)	0.3°C/W (2 x 0.6 in //)	0.55°C/W (2 device in //)	55°C
9.6 mΩ 1200V (simulated)	**9.6 mΩ 1 x device in HU3PAK**	0.2°C/W	0.6°C/W	0.8°C/W (one device)	80°C

Two devices in parallel provides significantly better thermal behavior than a single switch

*TIM used: 10 W/m*K - thermal conductivity - 0.8 mm

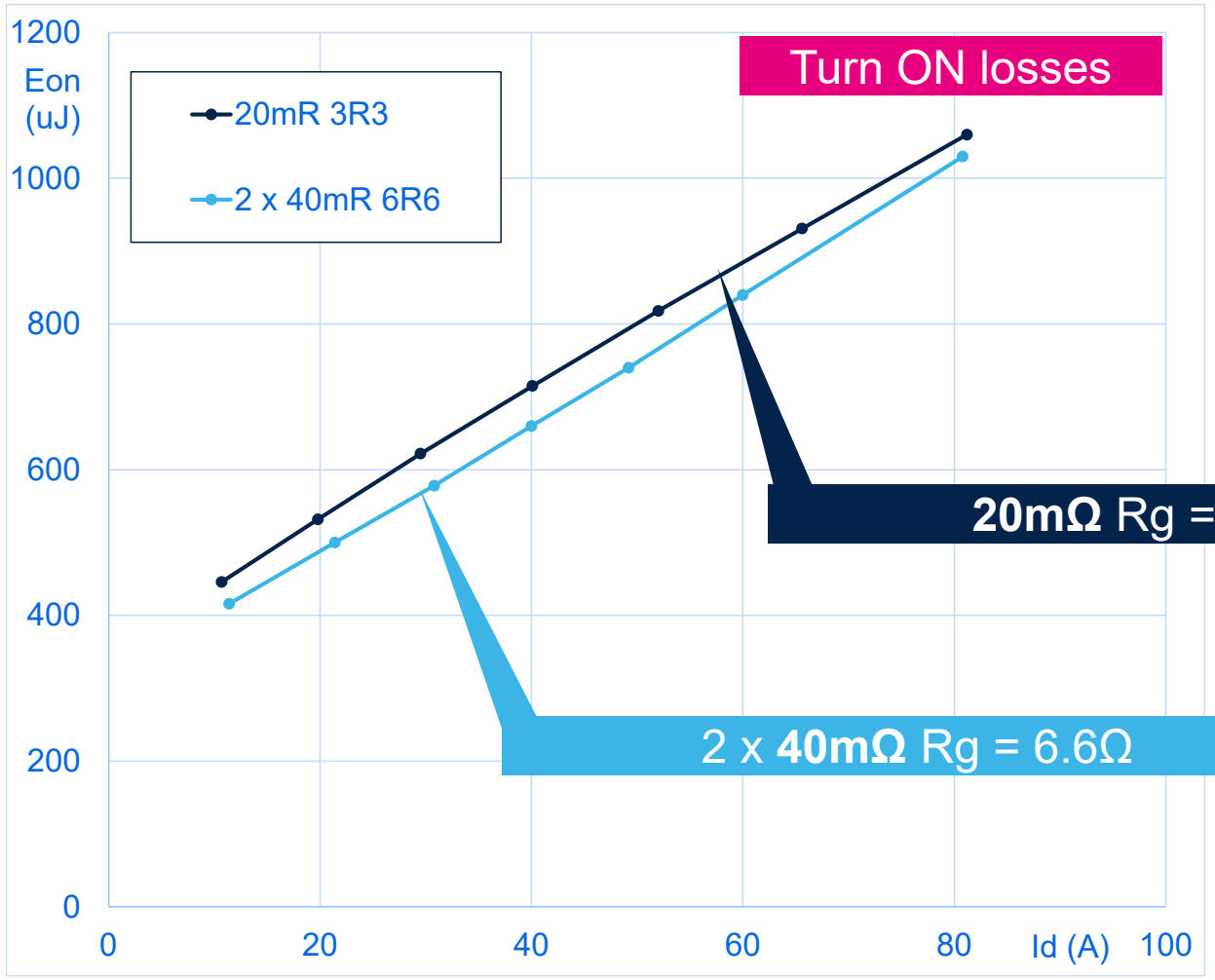
Results of best TIM material measurements
for HU3PAK

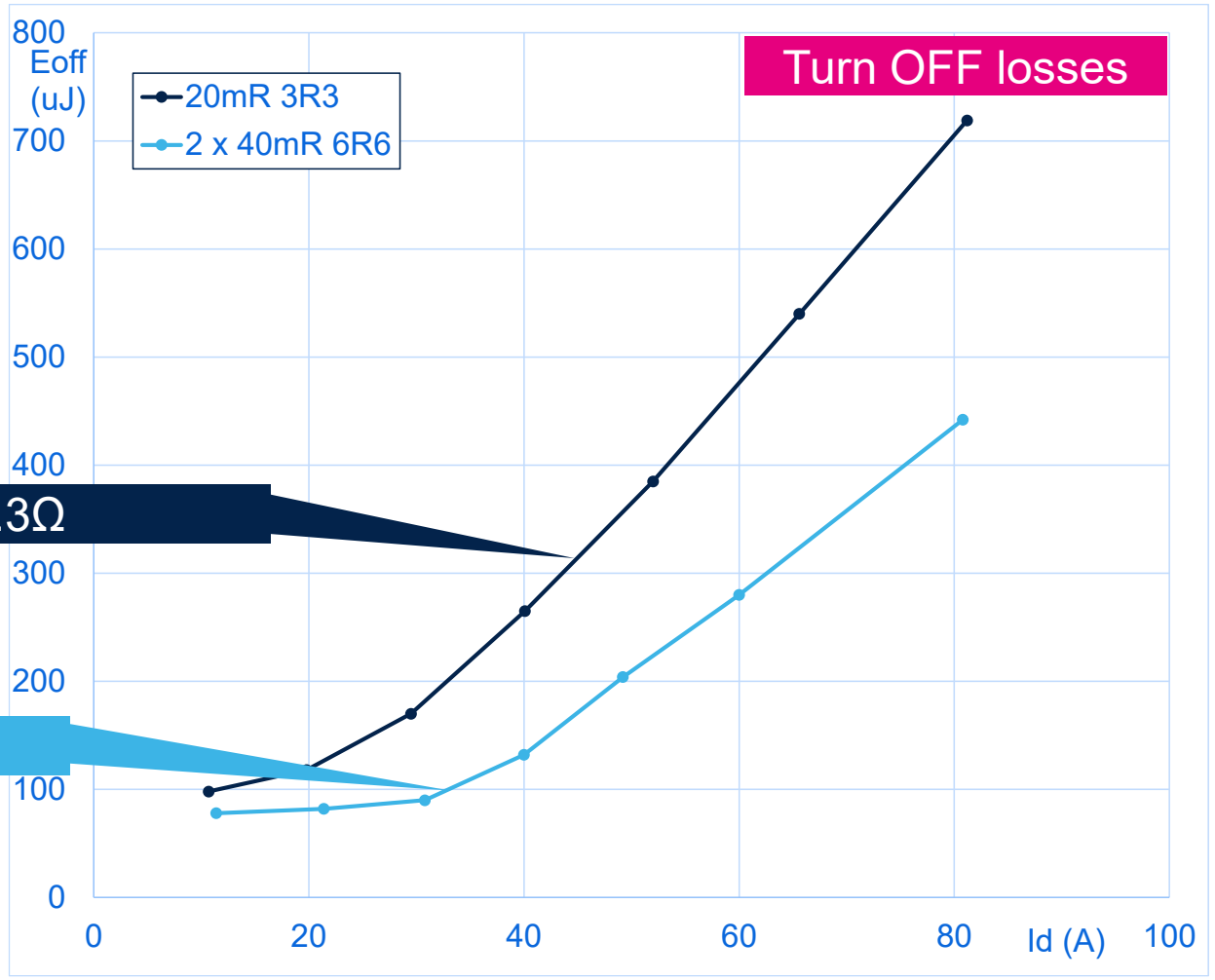
1) **0.32 K/W Gap-Filler pad – 0.7mm thickness**

2) **0.33 K/W Liquid Gap-Filler – 0.7mm thickness**

3) **0.35 K/W Al_2O_3 ceramics + Thermal paste + Counterplate – 1.0mm thickness**

Benefits of parallelization
2. Switching losses





20mΩ Rg = 3.3Ω

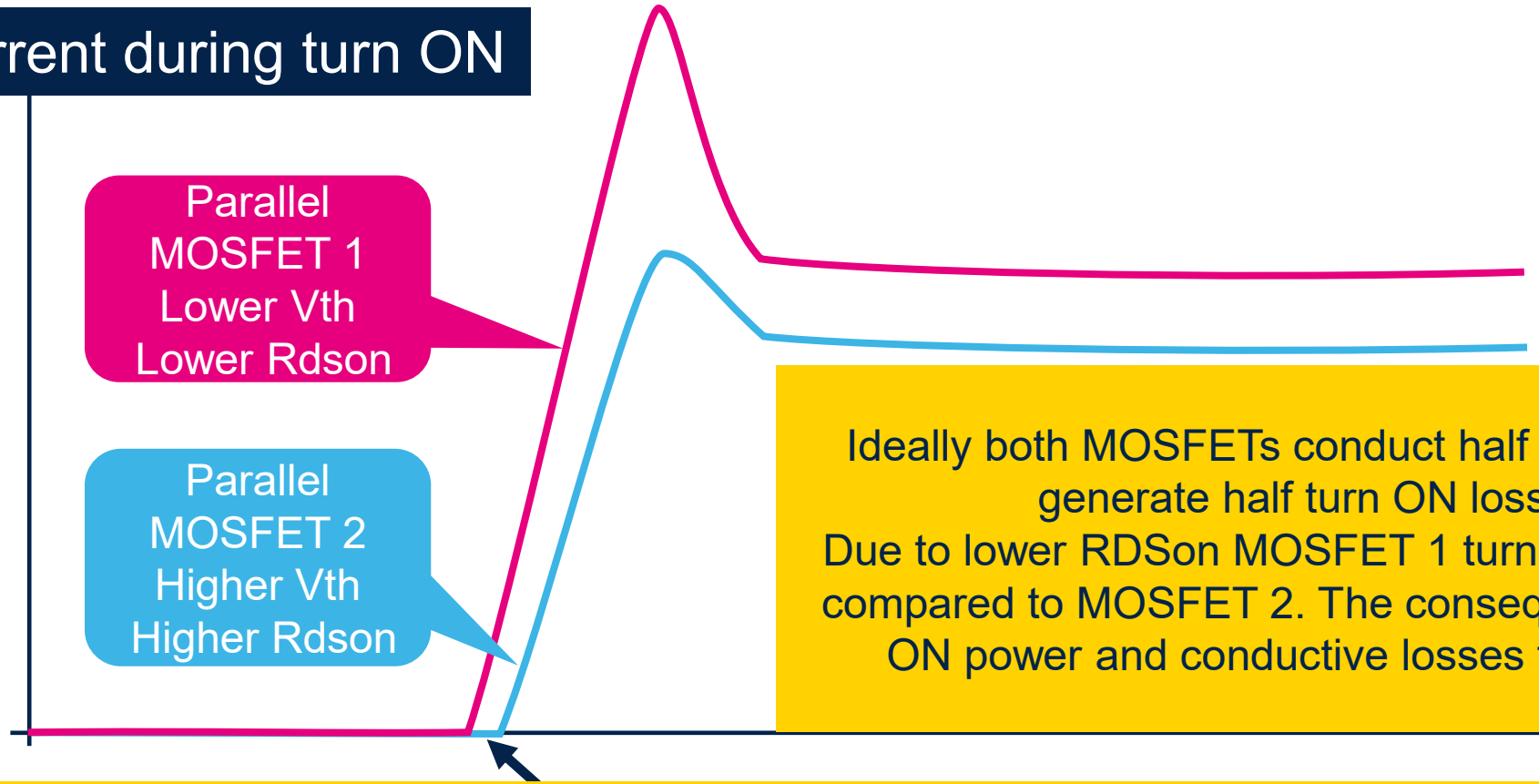
2 x **40mΩ** Rg = 6.6Ω

Comparing 2 devices in parallel and single device with comparable RDSon
2 devices will generate lower switching losses

Challenge

Vth and RDSon impact to switching losses
Two MOSFETs in parallel – issue explanation

Drain Current during turn ON



Ideally both MOSFETs conduct half of total current and generate half turn ON losses each.
Due to lower RDSon MOSFET 1 turn ON current is higher compared to MOSFET 2. The consequence is higher turn ON power and conductive losses than MOSFET 2.

Ideally both MOSFETs conduct half of total current and generate half turn ON losses each.
Due to lower Vth MOSFET 1 turn ON early compared to MOSFET 2. The consequence is the current through MOSFET 1 will be higher than expected and consequently will generates more turn ON power losses than MOSFET 2.

Challenge
Vth and RDSon difference

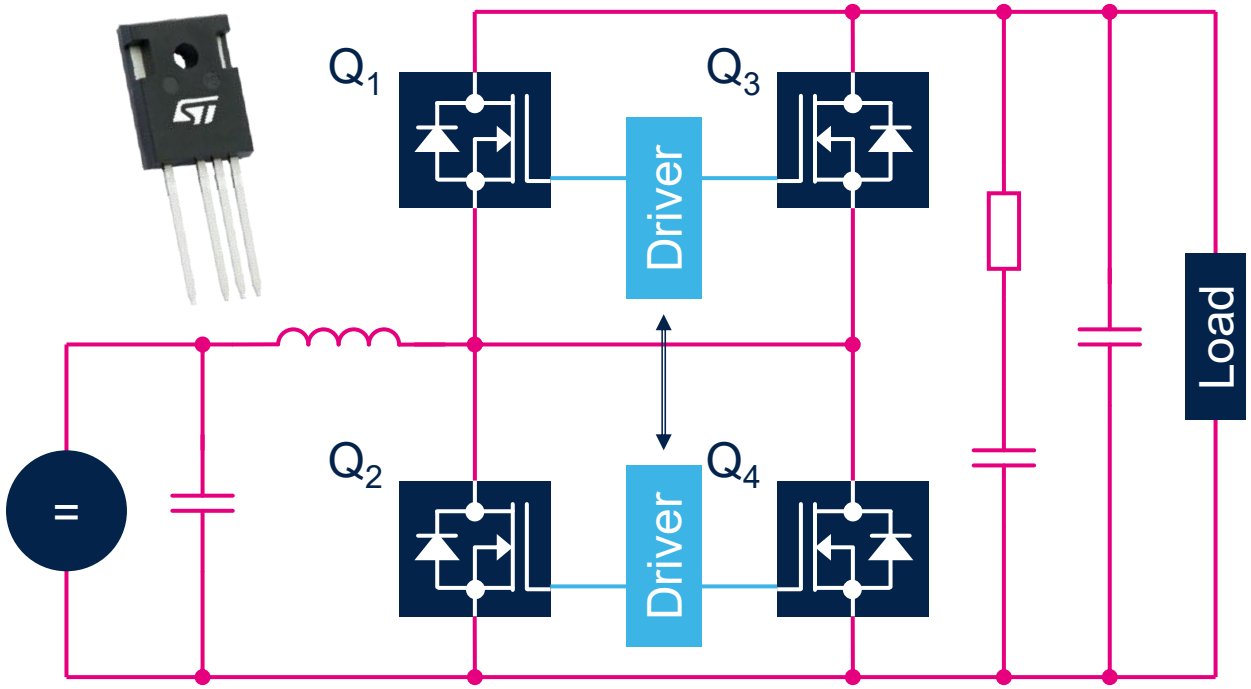
- Vth difference
  - Causes one device is turning ON/OFF earlier than other one thus conducting higher current during switching → This part generates higher switching losses
  - At higher temperature Vth is lower – it introduces positive feedback loop
- RDSon difference
  - Part with lower RDSon conducts more current. As conductive losses depends on the Irms square, this part generates more conductive losses
  - RDSon is higher at higher temperature – it introduces negative feedback loop
- Effect of unbalance can be also partly reduced by thermal “crosstalk”
  - it introduces negative feedback loop

ΔVth 350mV
ΔRdson 1.1mΩ

Practical example – Unbalanced Vth and RDSon

High Vth		Low Vth	
$R_{DS(on)}$ [mR]	$V_{GS(th)}$ [V]	$R_{DS(on)}$ [mR]	$V_{GS(th)}$ [V]
27.20	3.063	26.32	2.750

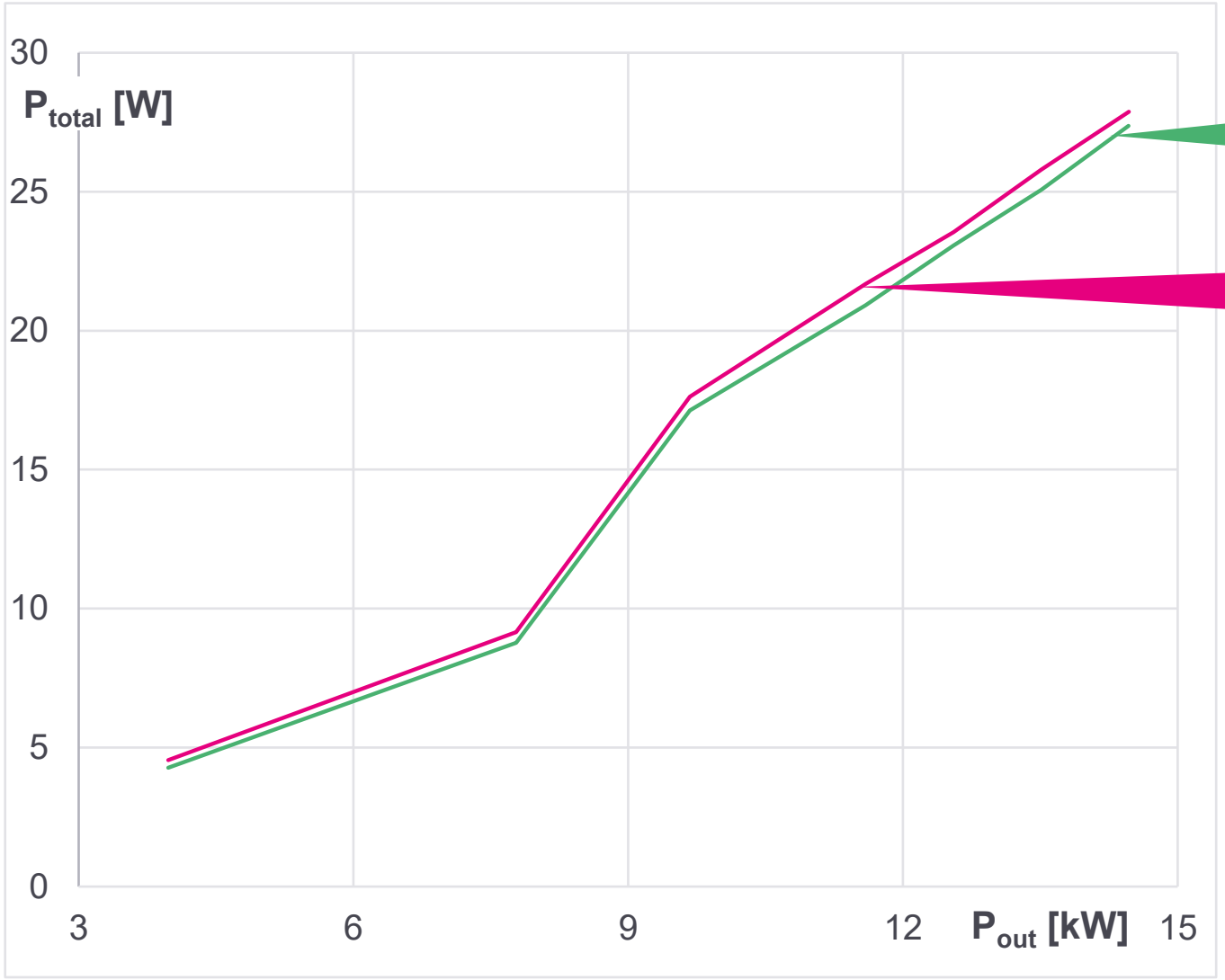
- **SiC MOSFET 27mΩ, 1.2kV,**
- **Vth** difference **– 350mV, ΔRDSon 1.1mΩ**
- Configuration of step-up converter
  - From 400 V_{DC} to 800 $V_{DC,}$ output up to 15kW
- All devices on same heatsink with thermal pads (electrically insulating)
  - Defined contact pressure to the heatsink
- Measuring both V_{GS} and V_{DS} with optical isolated probes
- Monitoring temperature of heatsink, heatsink under each MOSFET as well as temperature of case of each device



Monitoring especially low-side MOSFETs (Q_2, Q_4) as these are most stressed in this type of confugiration

ΔVth 350mV
ΔRDSon 1.1mΩ

Practical example – Unbalanced Vth and RDSon
Result



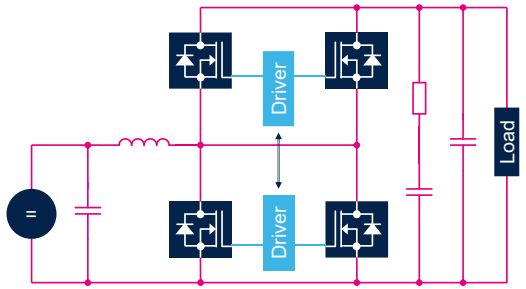
Power losses of one device for **ideal conditions**. Vth of both parts is similar.

Power losses for one device of **more stressed device** for **different Vth** (350mV).

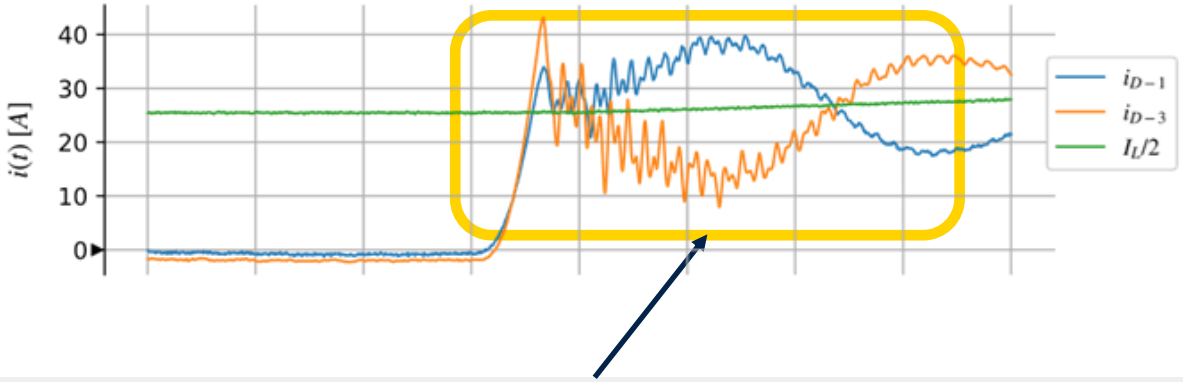
- One device power losses between **ideal** condition and **worse** case condition was **0.5W (2%)**

Layout impact – tests with HU3PAK
Comparison on signal level

ΔVth 250mV
SCT019HU120G3AG

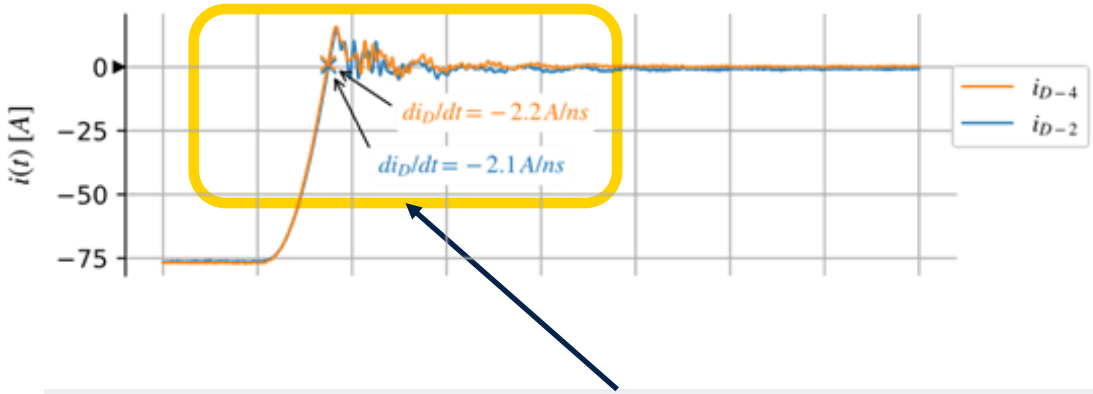


Tur ON – current waveform
Non ideal layout (2 layer)



Blue – Id through MOSFET 1
Orange – Id through MOSFET2
Significant unbalance and oscillation due to Vth difference and non ideal layout

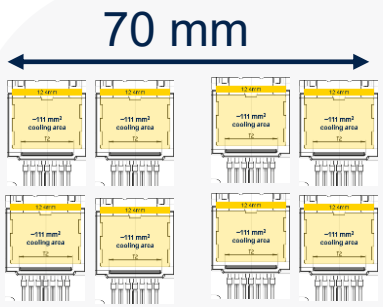
Tur ON – current waveform
Very good layout (4 layer)

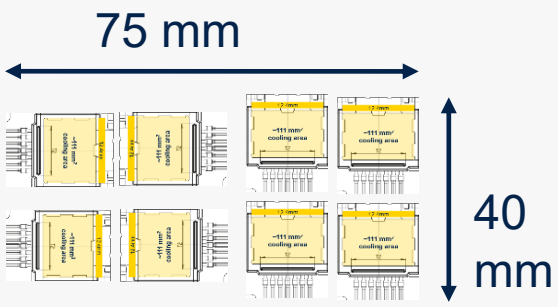


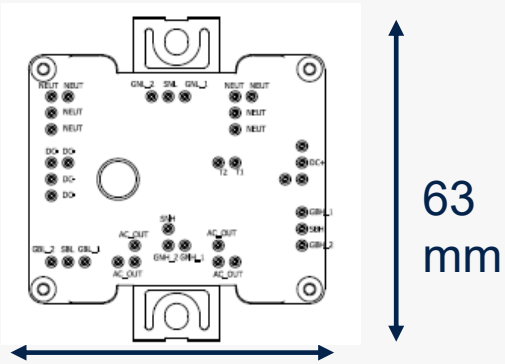
Blue – Id through MOSFET 1
Orange – Id through MOSFET2
Thanks good layout the currents are in similar tracks even Threshold difference

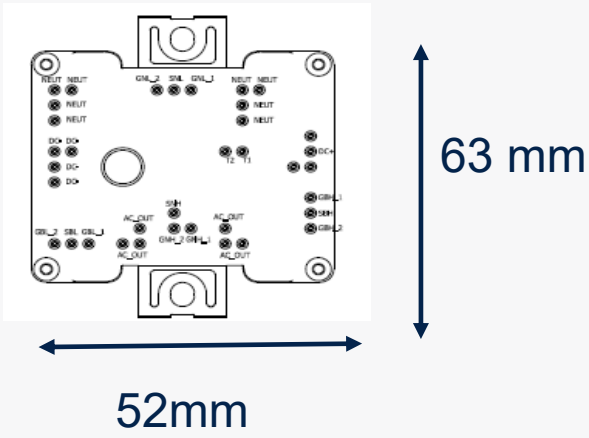
SiC HU3PAK vs Power Module
PCB Area layout examples

Discretes enable great flexibility vs design optimization





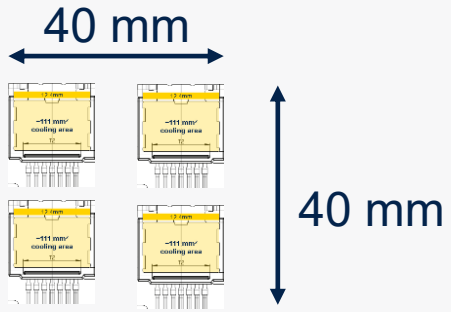


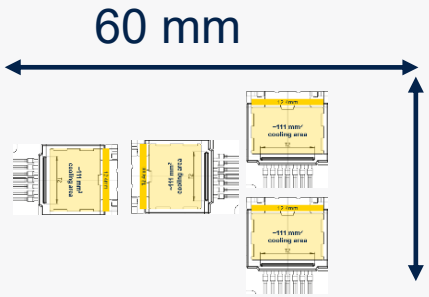


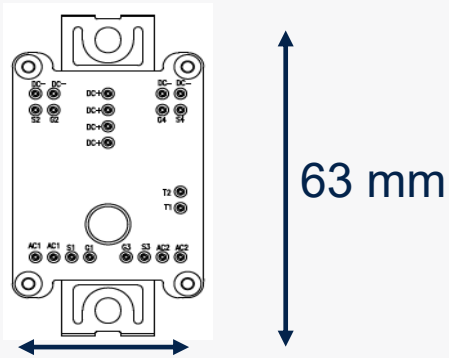
Full bridge
2 Devices in //

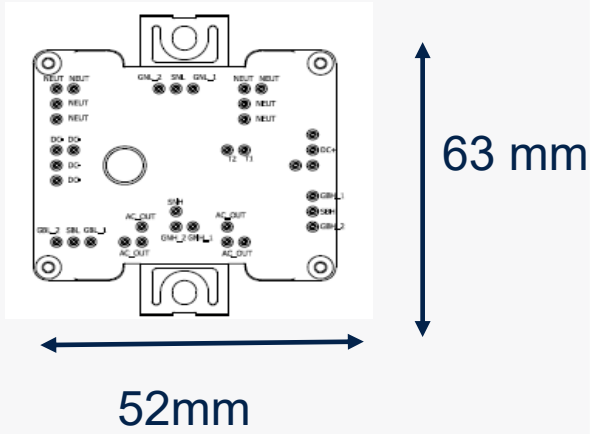
T-TYPE
2 Devices in //

Parallel MOSFETs - Optimized for thermal resistance









Full bridge
1 Devices /switch

T-TYPE
1 Devices /switch

Optimized for number of devices reduction (or interleaved solution)

Conclusion

Conclusion

- **Parallelization** allows to achieve **higher power transfer** thanks to:
  - Reduction of thermal resistance to heatsink allowing to reduce device temperature
  - Reduction of switching power losses (turn OFF)
- **Parallelization** allows **using discretes** for application typically covered by **power modules**
- Potentially Rth and Vth differences leads to different power - but
  - RDSon difference impact to conductive losses is naturally compensated by Rdsn vs thermal dependance
  - Vth difference (for presented example) – deviation between higher temperature device and ideal condition is in range of few %
  - The **good layout** (reduction of commutation loop) helps to reduce Vth impact to current unbalance

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