Selection and Optimization of Topside Cooling Options for Discrete SiC MOSFETs for High Power Density Applications

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Bodo's Wide Bandgap Event 2025

Making WBG Designs Happen

SiC

AOS SNAP SHOT

AOS is a designer, developer and global supplier of a broad range of power semiconductors, including Power MOSFETs, IGBTs, Power ICs, and TVS products. We develop advanced technologies and products to provide innovative power management solutions for our customers.

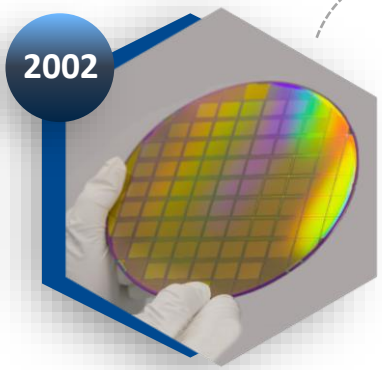
Core Competencies

- *Power Discrete, IC and Module solutions*
- *Advanced packaging with multi-chip integration competence*
- *In-house 8” fab in Oregon, USA*
- *Joint venture 12” fab in Chongqing, China*
- *High volume in-house AT and OSAT*

Founded	HQ	Employees	FY2022
2000, IPO 2010 (AOSL)	Sunnyvale, CA	2,451	Revenue $778M

AOS History

Found in Silicon Valley, CA



Co-produce world's 1st 8" LV MOSFET wafer

1st AT and OSAT factory in Shanghai

Released 1st PMIC

2nd AT and OSAT factory in Shanghai

IPO 2010 AOSL

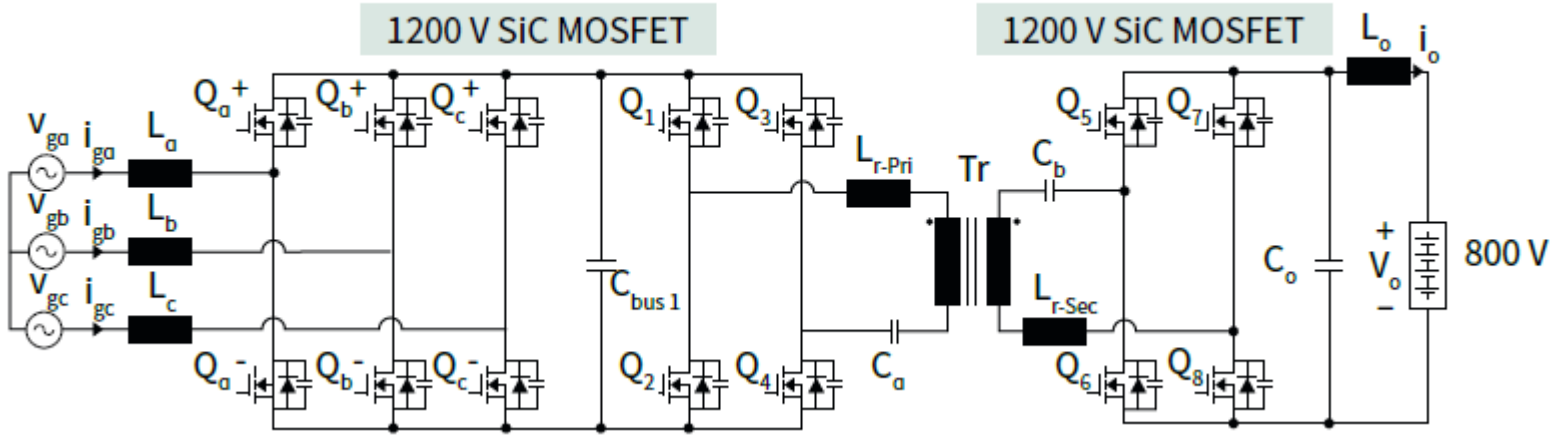
In-house 8" fab in Oregon, USA

Joint venture 12" fab in Chongqing, China

Released 1st 1200V SiC MOSFET

3rd OSAT factory in Malaysia, Thailand

Power Density Trends: OBC / Server



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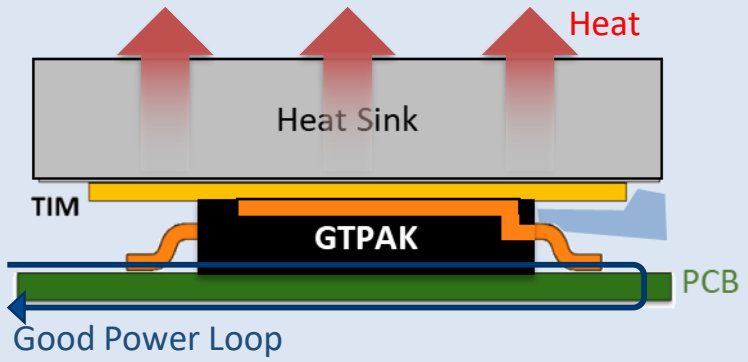
Through Hole	Surface Mount	Topside Cooled	Topside Cooled Module
• Power handling	• Low Profile	• Power handling	• Higher Power Density
• Known design	• Power density	• Power density	• Low Profile
• Large Heatsink	• Higher Rth	• Low Profile	• Assembly
• Through-hole assembly	• Reduced board routing	• Assembly Complexity	• Flexibility
			• Through hole board

AIR COOLING → LIQUID COOLING

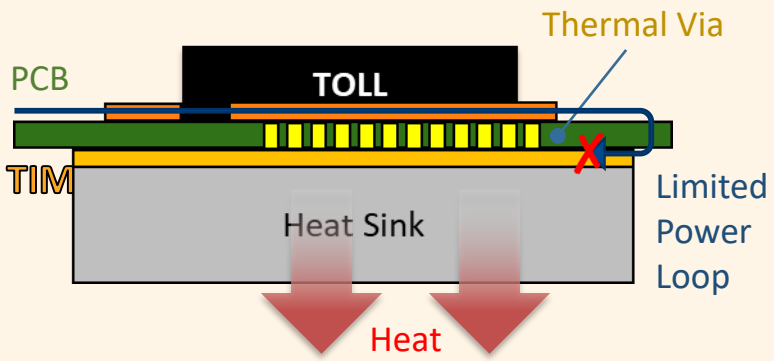
Topside Cooling Advantages

Example: GTPAK vs. Different TOLL PCB Assembly

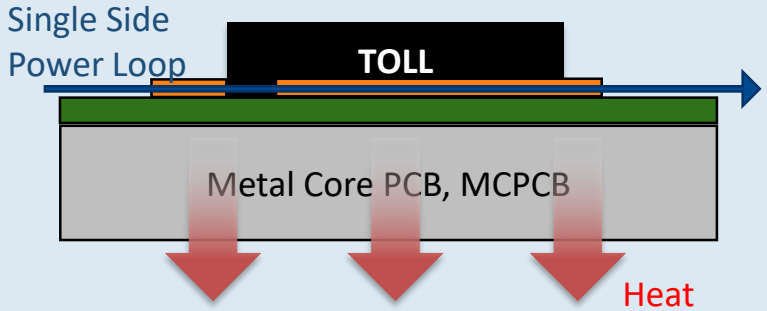
GTPAK FR4 PCB Assembly



TOLL FR4 PCB Assembly



TOLL MCPCB Assembly



Topside Cooling Advantages:

1. The optimum between thermal performance and system cost

   vs. "TOLL FR4 PCB Assembly": Similar system cost but 10% better thermal dissipation in MOSFET

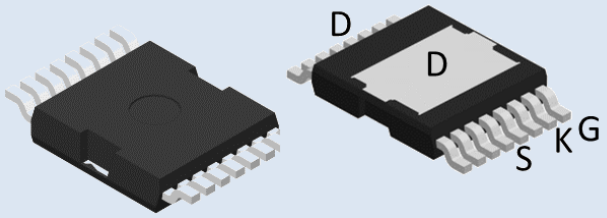
   vs. "TOLL MCPCB Assembly": Similar thermal performance, but lower PCB cost

2. Maximize PCB space for electric circuit optimization → Increase robustness and reliability.
3. Enhance board level reliability by absorbing the mechanical stresses with gull wing leads.
4. Perfectly matches with both air cooling and the increasing focused direct liquid cooling systems
5. Target applications including AI server, motor drive, solar power, and industrial power supplies.

High-Voltage SiC Topside Cooled Options

GTPAK / TOLT

- Footprint compatible with TOLT
- Material group I (>600V)
- 650V/750V
- Package creepage ~3.5 mm
- Extended > 5mm D-S creepage
  - [creepage dependent on TIM]

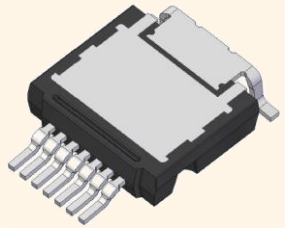


Size: 10mm x 15mm

Height: 2.3 mm

T2PAK / HU3PAK

- **T2PAK** pin-to-pin with HU3PAK
- 650V and 1200V Gen3
- Material Group I (>600V)
- Package creepage ~ 3.7mm
- Extended > 6.4mm D-S creepage
  - [creepage dependent on TIM]



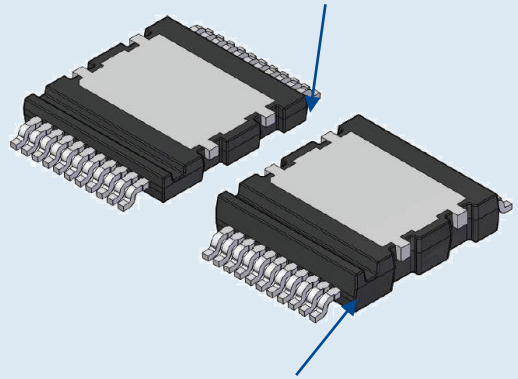
Size: 14mm x 18.58mm

Height: 3.5 mm

QDPAK

- JEDEC standard **QDPAK**
- 650V/750V/1200V+
- Material group I (>600V)
- Package creepage > 6mm

Height standard 2.3mm QDPAK



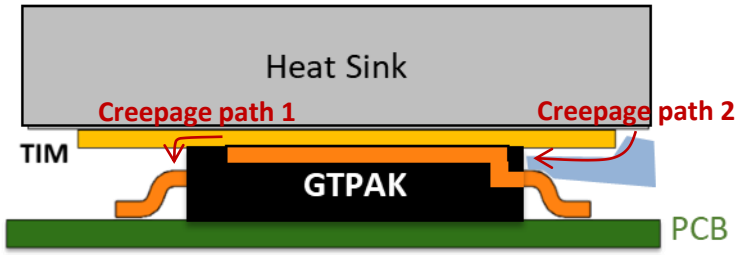
Height extended Creepage/Clearance 3.5mm

Size: 15mm x 21mm

Creepage Clearance Mold Compounds

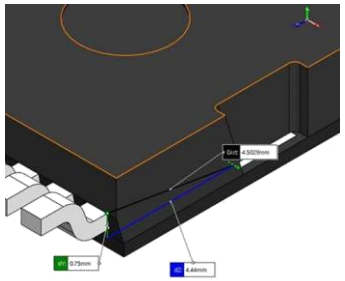
Creepage definition can be tricky

- Accept that TIM isolation is good enough?
  - → Path 1 is blocked by TIM (?)
  - → creepage path is now path 2 … otherwise



- Then need to consider: GTPAK
  - Pollution degree: Most applications PD II
  - Working voltage: 800VDC
  - Material Group: MC CTI = Material Group I

GTPAK has 5mm creepage - meets ~ 1kV Vrms



IEC 60664

Working voltage	Basic insulation and supplementary insulation						
	Pollution Degree 1	Pollution Degree 2			Pollution Degree 3		
	Material Group	Material Group			Material Group		
	I, II, IIIa or IIIb	I	II	IIIa or IIIb	I	II	IIIa or IIIb
50 V r.m.s. or d.c.	Use the CLEARANCE from the appropriate table	0,6 mm	0,9 mm	1,2 mm	1,5 mm	1,7 mm	1,9 mm
100 V r.m.s. or d.c.		0,7 mm	1,0 mm	1,4 mm	1,8 mm	2,0 mm	2,2 mm
125 V r.m.s. or d.c.		0,8 mm	1,1 mm	1,5 mm	1,9 mm	2,1 mm	2,4 mm
150 V r.m.s. or d.c.		0,8 mm	1,1 mm	1,6 mm	2,0 mm	2,2 mm	2,5 mm
200 V r.m.s. or d.c.		1,0 mm	1,4 mm	2,0 mm	2,5 mm	2,8 mm	3,2 mm
250 V r.m.s. or d.c.		1,3 mm	1,8 mm	2,5 mm	3,2 mm	3,6 mm	4,0 mm
300 V r.m.s. or d.c.		1,6 mm	2,2 mm	3,2 mm	4,0 mm	4,5 mm	5,0 mm
400 V r.m.s. or d.c.		2,0 mm	2,8 mm	4,0 mm	5,0 mm	5,6 mm	6,3 mm
600 V r.m.s. or d.c.		3,2 mm	4,5 mm	6,3 mm	8,0 mm	9,0 mm	10,0 mm
800 V r.m.s. or d.c.		4,0 mm	5,6 mm	8,0 mm	10,0 mm	11,0 mm	12,5 mm
1 000 V r.m.s. or d.c.		5,0 mm	7,1 mm	10,0 mm	12,5 mm	14,0 mm	16,0 mm

Linear interpolation is permitted between the nearest two points, the calculated spacing being rounded to the next higher 0,1 mm increment.

For REINFORCED INSULATION, the values for CREEPAGE DISTANCE are twice the values for BASIC INSULATION.

For glass, mica, ceramic or similar materials it is permitted to use minimum CREEPAGE DISTANCES equal to the applicable CLEARANCES.

Material Groups are classified as follows:

- Material Group I 600 ≤ CTI (Comparative tracking index)
- Material Group II 400 ≤ CTI < 600
- Material Group IIIa 175 ≤ CTI < 400
- Material Group IIIb 100 ≤ CTI < 175

The Material Group is verified by evaluation of the test data for the material according to IEC 60112 using 50 drops of solution A.

If the Material Group is not known, it can be determined by the test for the proof tracking index (PTI) as detailed in IEC 60112, OR Material Group IIIb can be assumed.

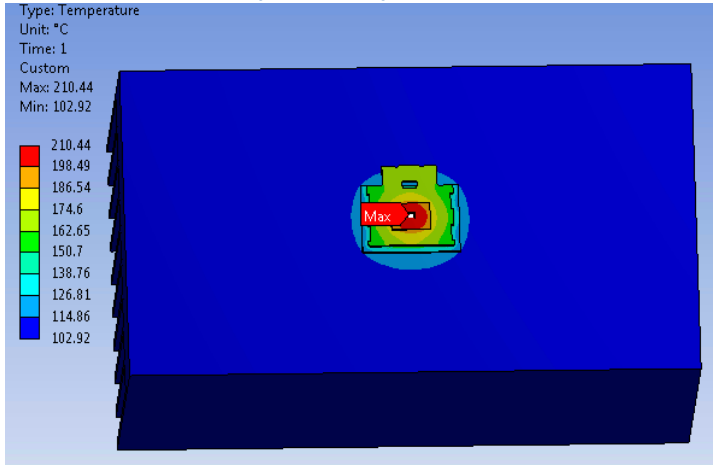
Large Topside Cooled Package Simulation

- **Compare HU3PAK type vs QDPAK type**
  - **Assume average heat transfer convection applied on the surface**
  - **Constant power dissipation applied to die**
  - **Very similar performance – Final package depends on customer needs**

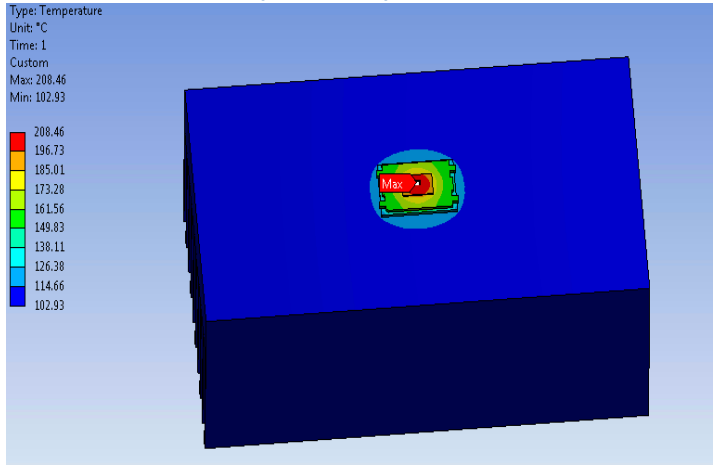
Summary of simulation

PKG Type (TIM conductivity)	QDPAK (3.5W/mK)	QDPAK (5W/mK)	HU3PAK (3.5W/mK)	HU3PAK (5W/mK)
Junction Temperature(°C)	228.4	207.8	220.2	210.4

HU3PAK Temp distribution-
SiC: 210.4°C.(TIM:5)

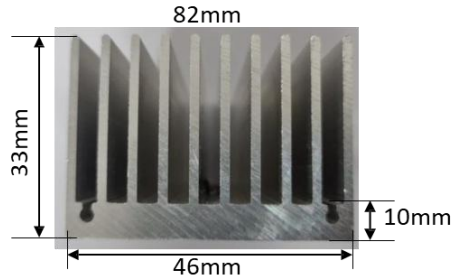


QDPAK Temp distribution
SiC: 207.8°C.(TIM:5)



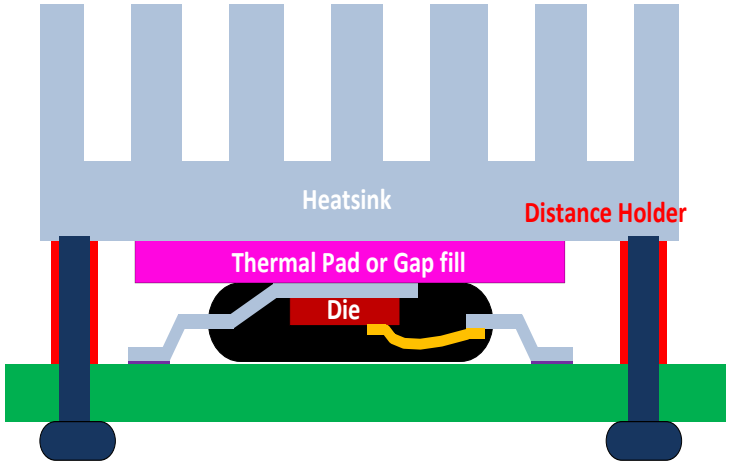
GTPAK vs QDPAK Power Optimization

- **When to choose GTPAK vs QDPAK**
- **Simulation setup: Consider 2 different thermal TIM systems**



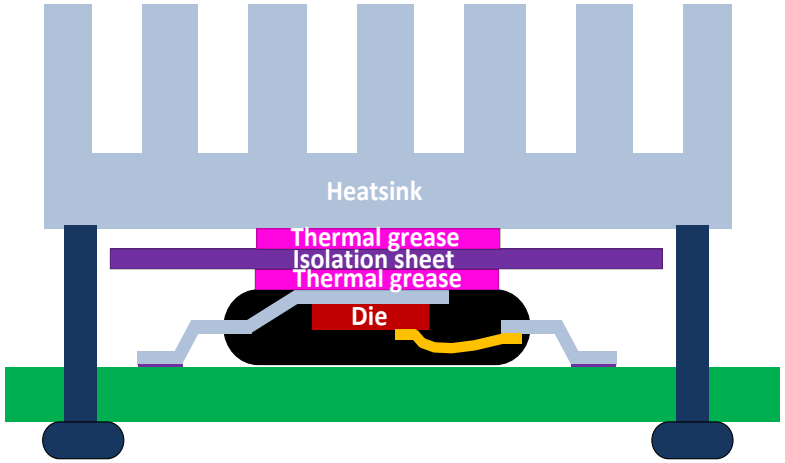
Option TIM1

Gap filler: λ~5.1W(mK), Thickness: 0.3mm

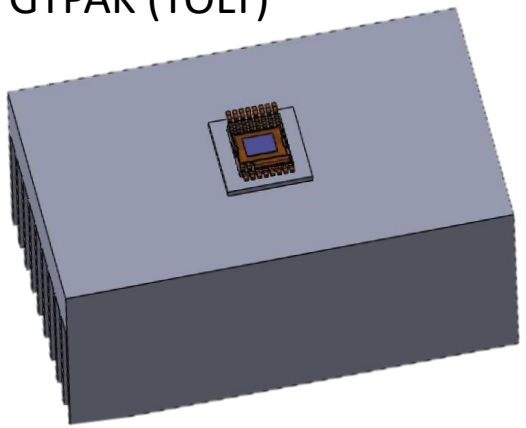


Option TIM2

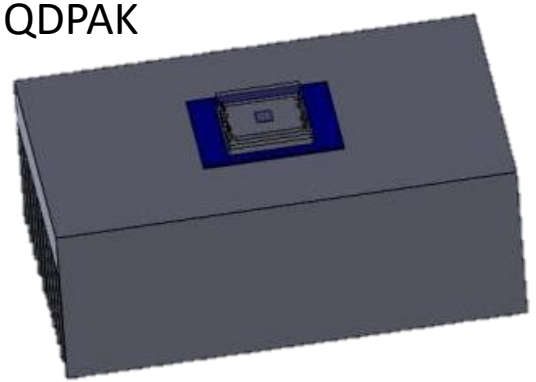
Option1: Isolation sheet + Thermal grease:
AIN's λ: 200W(mK), thickness: 0.5mm
2xThermal grease @ λ~ 5W(mK), thickness: 0.1mm



GTPAK (TOLT)



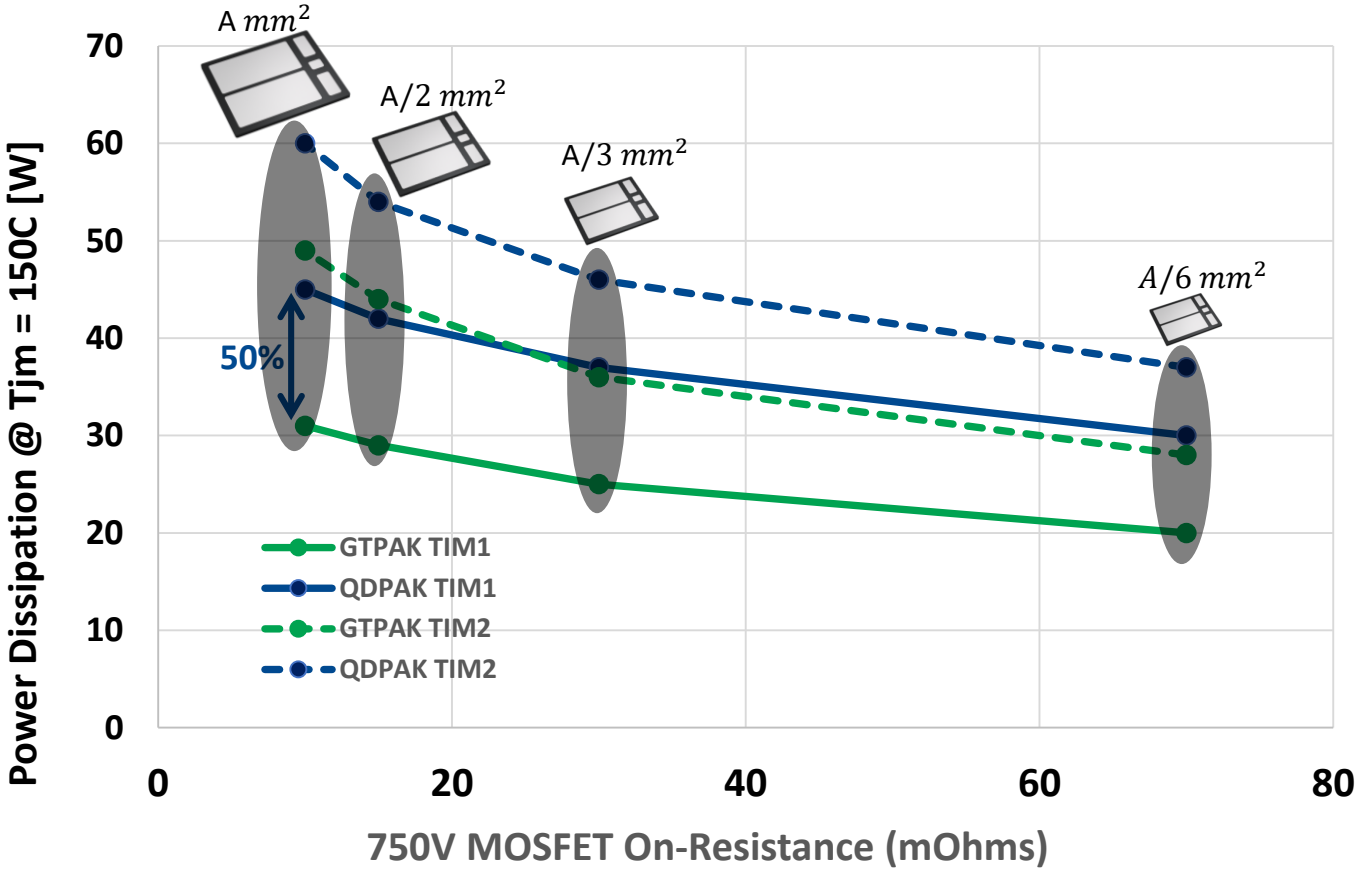
QDPAK



- **<u>Methodology</u>: Change die size → Increase power → Record Power at T_j= 150°C**

GTPAK vs QDPAK: 750V SiC MOSFET Power Simulations

- With TIM1: 50% higher power in QDPAK vs GTPAK for all die sizes
- With TIM2: Can get equivalent power with GTPAK over TIM1 in QDPAK
- With TIM2: Difference in GTPAK and QDPAK power output is ~ 20%



Thank You