Advanced SiC technology for automotive applications

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Bodo's Wide Bandgap Event 2025

Making WBG Designs Happen

SiC

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starpower

Outline

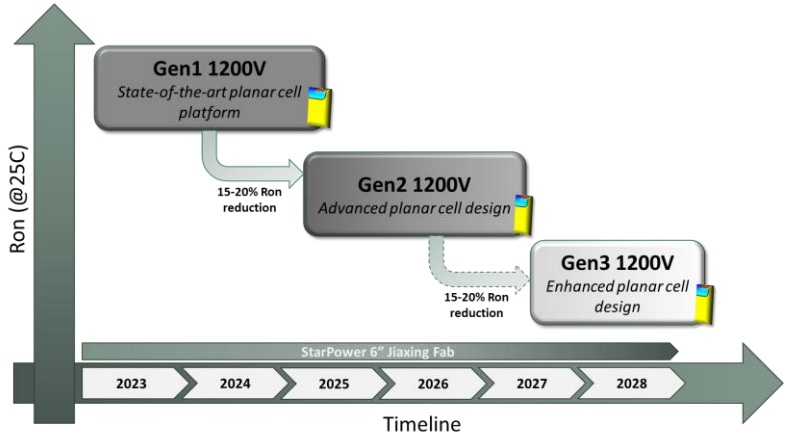
- Introduction
- StarPower SiC technology
- Reliability qualification
- StarPower SiC portfolio
- Conclusions

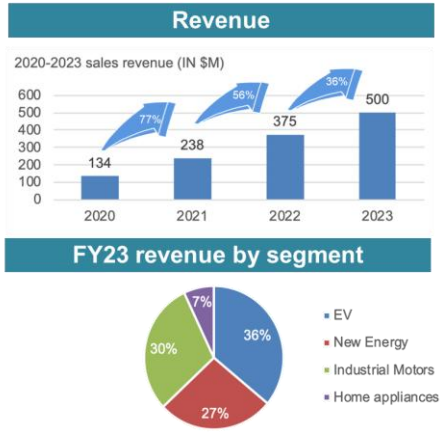
StarPower general introduction

StarPower, Jiaxing (Headquarter)

Main R/D center and sales office are located in Jiaxing, China. Total employee are 900+.

Mainly focus on low power to high power IGBT modules and **SiC power modules**.
There are 3 production lines with clean room areas of 6000 m2 and labs with 3000 m2.

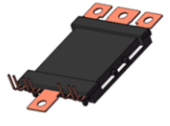




SiC modules for automotive traction

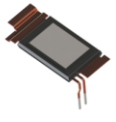
P6 module

Part Number	Power	Voltage
MD29HTC120P6HE	250kW	800V
MD22HTC120P6HET	300kW	800V
MD17HTC75P6HE	250kW	400V



N5/N6 module

Part Number	Power	Voltage
MD17HFC75N5H	250kW	400V
MD13HFC75N5H	300kW	400V
MD29HFC120N6H	250kW	800V
MD22HFC120N6H	300kW	800V

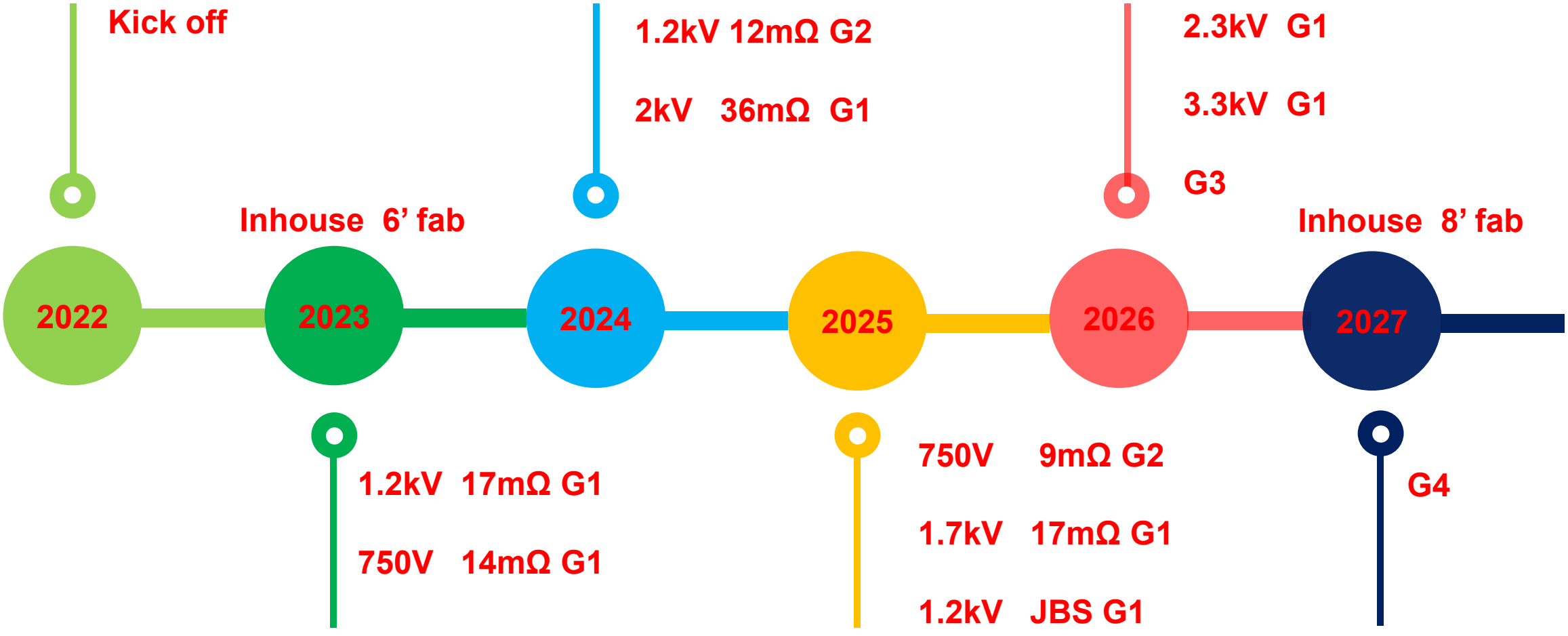


T6 module

Part Number	Power	Voltage
MD88C12T6	80kW/unit	800V
MD67C12T6	90kW/unit	800V
MD50C75T6	80kW/unit	400V

StarPower inhouse SiC fab

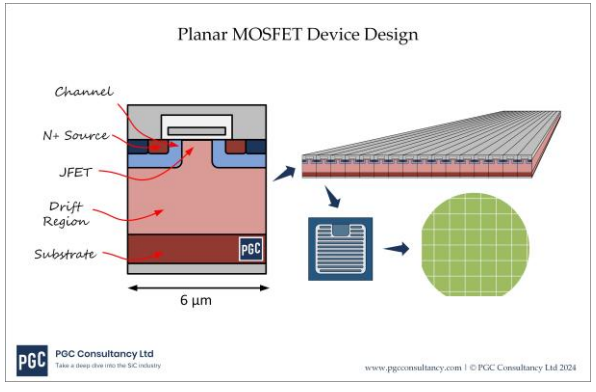
StarPower SiC power device development

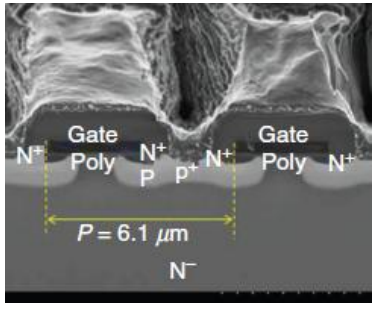


Design of the main cell: planar vs. trench

Planar cell

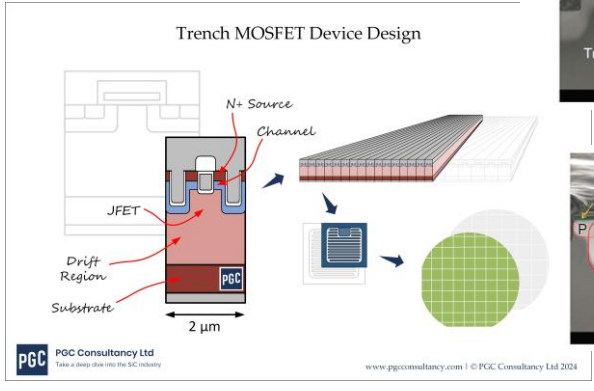
- Channel is lateral and sits just below the surface.
- In the low voltage range (≤1200V), the channel and JFET contribute significantly to the overall static losses.
- A good way to drive down the Ron values is to reduce the pitch -> this approach will hit a limit at some point.
- Current cell pitch values are around 4-6um.

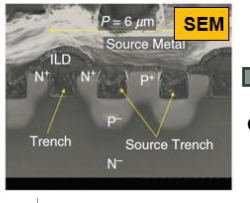




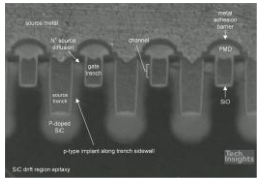
Trench cell

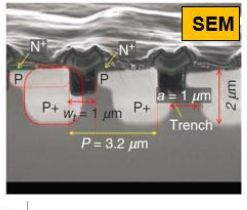
- Channel is vertically oriented.
- The pitch can be smaller (around 3um) than in planar. Increased channel density can result in the die being made smaller ->better yield.
- Special measures need to be taken to protect the trench corners, more complex processing.

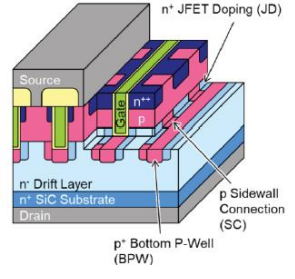




Gen3 to Gen4







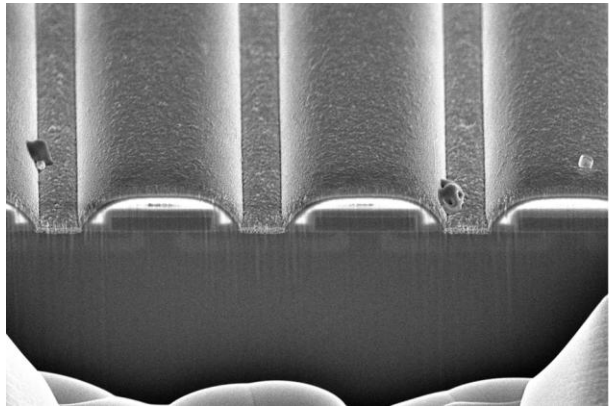
Both designs will probably co-exist for a while.

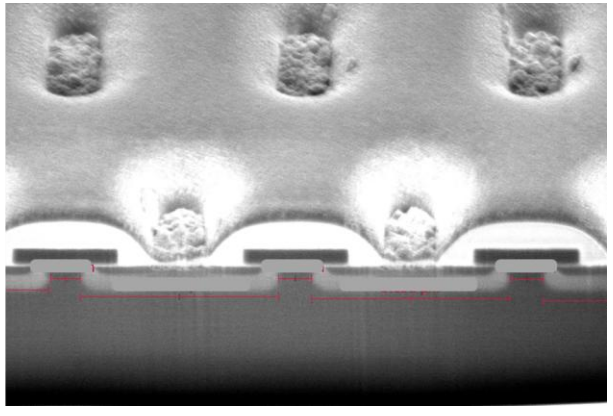
https://www.pgcconsultancy.com/post/trench-warfare-a-sic-battleground
https://www.techinsights.com/blog/rohm-gen-4-technical-review
A. Adan et al., "The Current Status and Trends of 1,200-V Commercial Silicon-Carbide MOSFETs", IEEE POWER ELECTRONICS MAGAZINE, June, 2019, p. 36
https://www.advance.mitsubishielectric.com/advance/pdf/2022/179_TR6.pdf

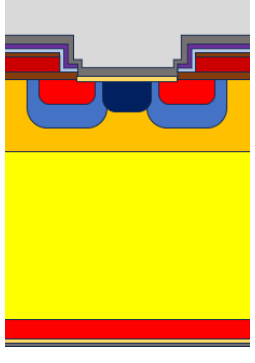
Design of the main cell: challenges as the cell pitch size shrinks

Notes

- Litho tool capability: with below 100nm overlap.
- CD around 300nm.
- Optimization of Inter Layer Dielectric (ILD) – good step coverage.
- Optimization Ohmic contact formation.
- Optimization of top metal stack deposition.
- Careful considerations should be applied for the Crss and Ciss capacitances.
- Design of the p+ in the third dimension.
- Short channel effects need to be considered carefully.
- Stripe vs cellular (hex/square) cells – special attention should be applied when moving from stripe to cellular design.







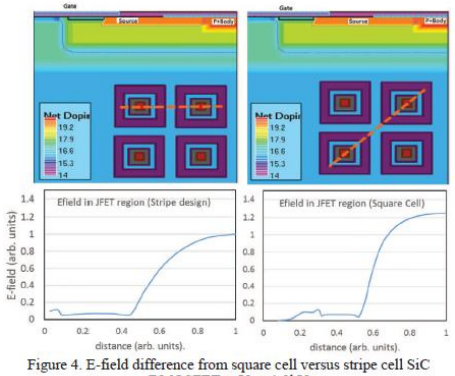
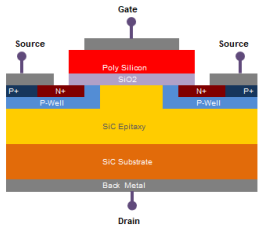


Figure 4. E-field difference from square cell versus stripe cell SiC DMOSFET at V_{DS}=1.2kV

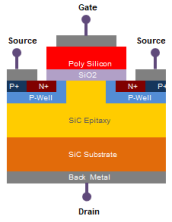
P. Losee et al, SiC MOSFET Design Considerations for Reliable High Voltage Operation, IEEE International Reliability Physics Symposium (IRPS), 2017, p. 2A-2.1

StarPower leading SiC chip technology – state-of-the-art benchmarking



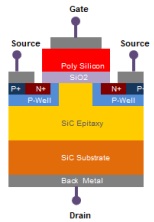
Gen1

Planar gate, strip cell



Gen2

Compact planar gate enhanced strip cell



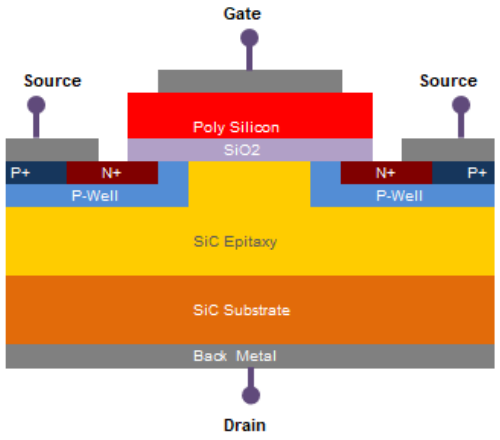
Gen3

Advanced planar gate enhanced strip cell

1200V MOSFET	Technology	RSP(25C)	RSP(175C)2	VTH（V）	Ciss/Crss Ratio	Tjmax (C)
StarPower Gen2E@2024	Planar	2.3	4.1	2.5	800	185
Competitor 1	Planar	2.3	4.35	2.5	420	175
Competitor 2	Planar	2.1	4.3	2.8	1100	175
Competitor 3	Trench	2.4	4.6	4.2	270	175
Competitor 4	Planar	2.3	4.35	2.5	500	185
Competitor 5	Trench	2.2	4.8	3.1	330	175

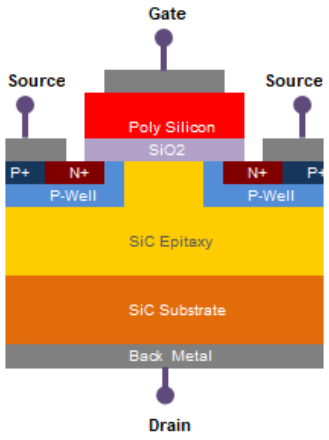
StarPower SiC chip technology evolution

Technology	Cell Structure	Vgs(V)	Vth (V)	RSP(25C) (mohm.cm^2)	RSP(175C) (mohm.cm^2)
1.2KV G1	Planar	15	2.5	3.1	5.3
1.2KV G2	Compact planar	15	2.5	2.7	4.7
1.2KV G2ET	Compact planar	18	2.7	2.3	4.1



Gen1

Planar gate, stripe cell design



Gen2/ Gen2ET

Compact planar gate, enhanced stripe cell design

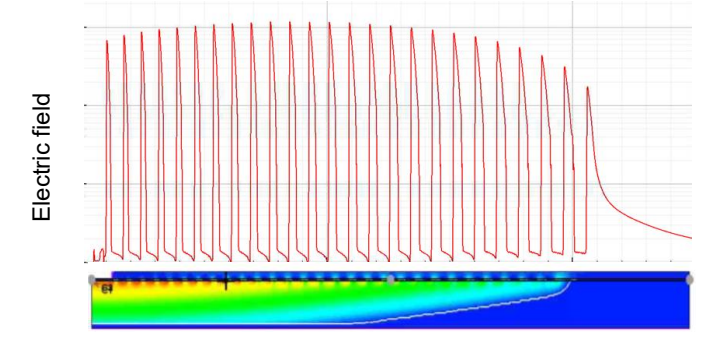
- **The Gen2/Gen2ET retains the planar gate structure of the Gen1 platform, continuing the high reliability and robustness of the Gen1 mass-production platform.**
- **Gen2/Gen2ET uses a higher-density cell design, resulting in a 13% and 26% reduction in on-resistance compared to Gen1, respectively, significantly reducing conduction losses and improving current output capability.**
- **Gen2/Gen2ET's improved cell design significantly reduces switching capacitance, thereby reducing switching losses.**
- **Gen2/Gen2ET also utilizes an enhanced HV-H3TRB solution to ensure device lifespan in high-temperature and high-humidity environments.**

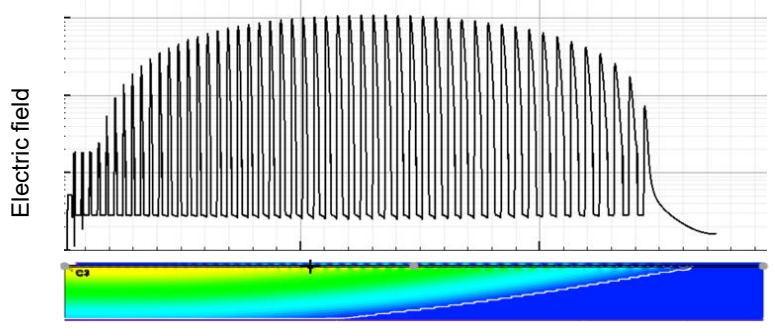
Design of the edge termination towards enhanced reliability

Notes

- The degradation of SiC devices under high temperature and high humidity conditions is related to excessive/non-optimized electric fields in the edge termination area.
- Electric field in the edge termination is designed towards ensuring required reliability levels.
- The edge termination design must be optimized together with the passivation layers used on top (what material/stack, how thick, surface cleaning and processing).

Electric field distribution at the SiC/passivation interface





Inclusion of DGS, DRB and Dynamic H3TRB in AQG 324

Notes

- AQG324 - an industry guideline based on best practices and cooperative requirement engineering alignment through the automotive supply chain for power electronic converter units.
- Dynamic Gate Switching (DGS) to test Gate Switching Instability (GSI)
  - Drift of Vth or RDSon greater than 20% are defined as failure.
- Evaluate dV/dt effects at chip and module level.
- Dynamic Reverse Bias (DRB)
  - Dynamic reverse bias (DRB) test should be carried out as technology qualification on chip-level.
  - The scope of the data sheet parameter drift analyses must be agreed with the customer (BV and Vth).
- Dynamic H3TRB
  - Dynamic H3TRB testing is an additional generic chip robustness test for the module technology.
  - The scope of the data sheet parameter drift analyses must be agreed with the customer.

Figure 9.3: Explanation of test $V_{GS}(t)$

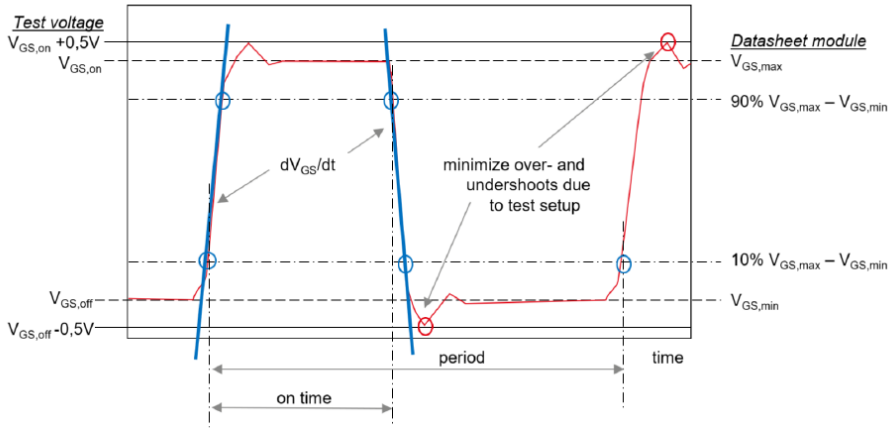
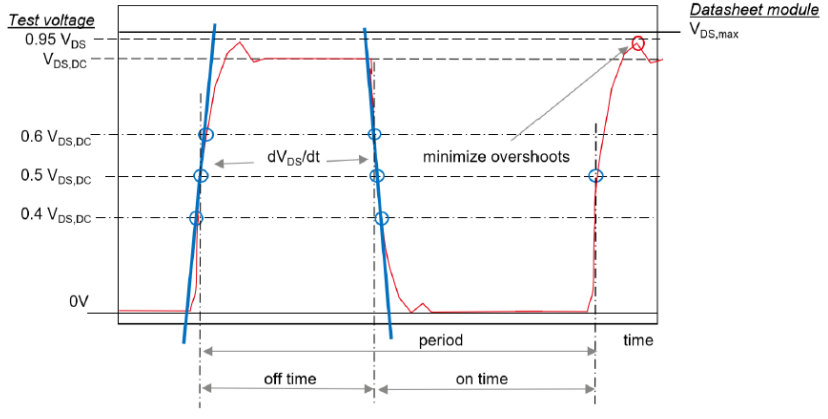
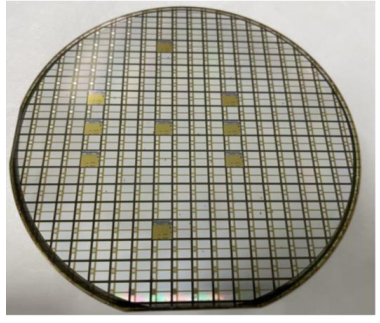


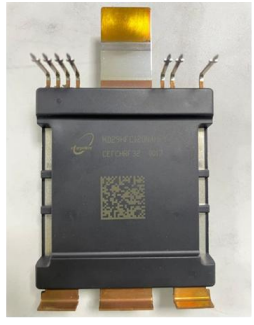
Figure 9.4: Explanation of test $V_{DS}(t)$



SiC chip reliability qualification – AEC-101 and AQG324



Chip Qualification



Module Qualification

Items	Stress conditions	Sample	Status	Completion date
HTRB	175℃, 80%V_{DS}, 1000h	3x77	PASS	Done
HTGB+	175℃, V_{GS}=+22V, 1000h	3x77	PASS	Done
HTGB-	175℃, V_{GS}=-8V, 1000h	3x77	PASS	Done
H3TRB	85℃, 85%RH, V_{DS}=80V, 1000h	3x77	PASS	Done
HAST	130℃, 85%RH, V_{DS}=42V, 96h	3x77	PASS	Done
HV-H3TRB	85℃, 85%RH, V_{DS}=960V, 1000h	3x77	PASS	Done
PCsec	75℃-175℃, ton=1.5s, 150k cycles	6	PASS	Done
PCmin	75℃-175℃, ton=15s, 25k cycles	6	PASS	Done
TS	-40℃~125℃, 1000cycles	6	PASS	Done
HTS	125℃, 1000h	6	PASS	Done
LTS	-40℃, 1000h	6	PASS	Done

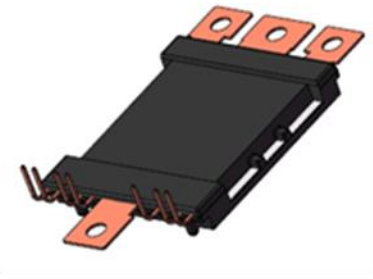
Items	Stress conditions	Sample	Status	Completion date
DGS	Vgs=+22V/-8V, Vdd=0V, f=10kHz,duty=50%, >10^{11}cycles	6	PASS	Done
DRB	Vgs=-8V, Vdd=960V, f=50kHz, duty=50%, >10^{11} cycles	6	PASS	Done
HTFB	Vgs=-4V, Isd=20A	6	PASS	Done
TDDB	175℃, TTF	3x40	PASS	Done
ARB	1400V, 175℃, 1000h	3x27	PASS	Done
ESD-HBM		1x30	PASS	Done

Items	Stress conditions	Sample	Status	Completion date
HTRB	185℃, 80%V_{DS}, 200h	3x77	PASS	Done
HTGB+	185℃, V_{GS}=+22V, 200h	3x77	PASS	Done
HTGB-	185℃, V_{GS}=-8V, 200h	3x77	PASS	Done
TDDB	185℃, TTF	3x40	PASS	Done
ARB	1400V, 185℃, 200h	3x27	PASS	Done

StarPower SiC MOSFET Module Market Application

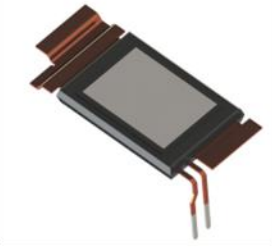
P6 module

Part Number	Power	Voltage
MD29HTS120P6HE	250kW	800V
MD22HTS120P6HET	300kW	800V
MD17HTS75P6HE	250kW	400V



N5/N6 module

Part Number	Power	Voltage
MD17HFS75N5H	250kW	400V
MD13HFS75N5H	300kW	400V
MD29HFS120N6H	250kW	800V
MD22HFS120N6H	300kW	800V



T6 module

Part Number	Power	Voltage
MD88S12T6	80kW/unit	800V
MD67S12T6	90kW/unit	800V
MD50S75T6	80kW/unit	400V

Scania

SAIC IM

AVATR

XiaoMi Ultra

Beijing SUV

FAW

Stellantis

AUDI PPE

Conclusions

- State-of-the-art SiC planar MOSFET technology
- Chip design, process control towards enhanced reliability
- Diverse range of product portofolio